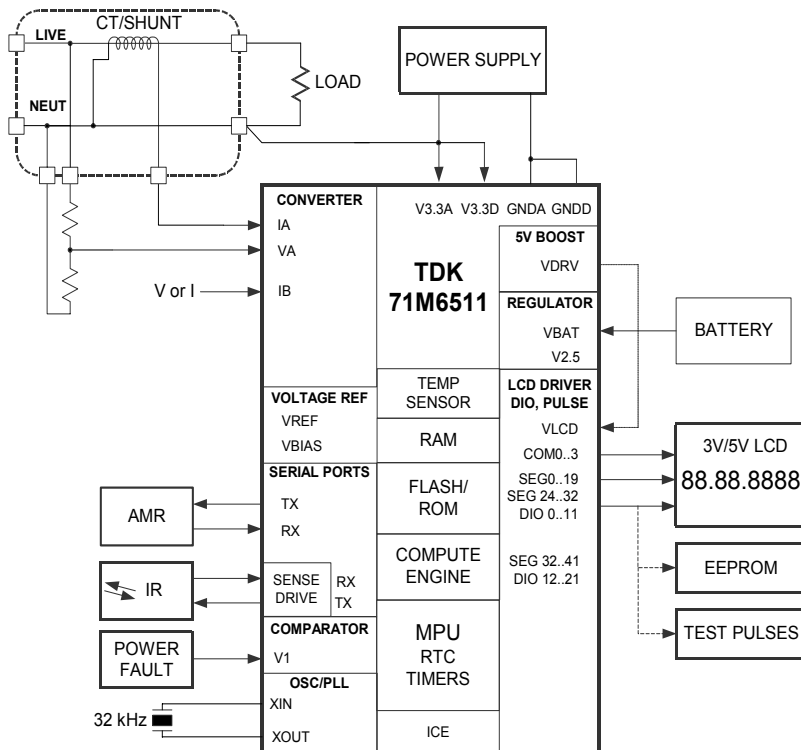


GENERAL DESCRIPTION

The TDK 71M6511 is a highly integrated SOC with an MPU core, RTC, FLASH and LCD driver. TDK's patented Single Converter Technology™ with a 22-bit delta-sigma ADC, 3 analog inputs, digital temperature compensation, precision voltage reference and 32-bit computation engine supports a wide range of residential metering applications with very few low-cost external components. A 32kHz crystal timebase for the entire system and Internal battery backup support for RAM and RTC further reduce system cost. The IC supports 2-wire and 3-wire single-phase residential metering along with tamper-detection mechanisms.

Maximum design flexibility is supported with multiple UARTs, I²C, power fail comparator, 5V LCD charge pump, up to 12 DIO pins and in system programmable FLASH which can be updated with data or application code in operation. Easy conversion to ROM offers unprecedented cost structure for high volume applications.

A complete array of ICE and development tools, programming libraries and reference designs enable rapid development and certification of TOU, AMR and Prepay meters that meet worldwide electricity metering standards.



FEATURES

- < 0.1% Wh accuracy over 3000:1 range (71M6511H version)
- < 0.5% Wh accuracy over 3000:1 range (71M6511 version)
- Exceeds IEC62053 / ANSIC12.20 standards
- Voltage reference < 10ppm/°C spec (71M6511H version), < 50ppm/°C (71M6511 version)
- Three sensor inputs—VDD referenced
- Digital temperature compensation
- 22-bit delta-sigma ADC
- Independent 32-bit compute engine
- Low jitter Wh and VARh pulse outputs
- 40-70Hz line frequency range
- CT Phase compensation ($\pm 7^\circ$)
- Battery backup for RAM and RTC
- 22mW @3.3V, 7.2 μ W battery backup
- Flash memory option with security
- 8-bit MPU (80515), 1 clock cycle per instruction
- Integrated ICE for MPU debug
- High speed SSI serial output
- RTC for time of use functions
- Two event counter/timers
- Watchdog timer, power fail monitor
- LCD driver (up to 128 pixels)
- Up to 12 general purpose I/O pins
- 32kHz timebase for RTC, CE, and MPU
- 64kB FLASH or ROM, 7kB total RAM
- Two UARTs for IR and AMR
- Third software UART via DIO pins
- 64-lead LQFP package
- Lead Free package option

Table of Contents

GENERAL DESCRIPTION	1
FEATURES.....	1
FUNCTIONAL DESCRIPTION.....	6
Digital Computation Engine (CE)	8
80515 MPU Core	11
Address.....	11
Interrupt	12
Internal Resources.....	12
Memory.....	14
I/O Peripherals.....	14
Digital I/O	16
EEPROM Interface	17
LCD Drivers	18
Optical Interface.....	15
Synchronous Serial Interface (SSI).....	18
SSI SIGNAL	19
System Timing Summary.....	20
Fault and Reset Behavior	21
Battery Operation/Power Save Modes.....	21
Watchdog Timer	22
Program Security	23
Voltage Reference	23
Application Information	24
I/O RAM DESCRIPTION – Alphabetical Order	25
I/O RAM MAP – In Numerical Order	33
CE Interface Description	35
Fundamental Power Measurement Variables	38
Instantaneous Power Measurement Variables	38
Other Measurement Parameters	39
Temperature Measurement	39
Pulse Generation.....	41
Current Shunt Variables	42

CE Calibration Parameters	43
ELECTRICAL SPECIFICATIONS	44
ABSOLUTE MAXIMUM RATINGS	44
RECOMMENDED EXTERNAL COMPONENTS	44
RECOMMENDED OPERATING CONDITIONS	45
PERFORMANCE SPECIFICATIONS	45
LOGIC LEVELS	45
COMPARATORS	45
SUPPLY CURRENT	46
VREF, VBIAS	46
2.5V VOLTAGE REGULATOR	47
ADC CONVERTER, VDD REFERENCED	47
CRYSTAL OSCILLATOR	47
OPTICAL INTERFACE	48
TEMPERATURE SENSOR	48
LCD BOOST	48
LCD DRIVERS	48
RTC	48
TIMING SPECIFICATIONS	49
RAM AND FLASH MEMORY	49
FLASH MEMORY TIMING	49
EEPROM INTERFACE	49
RESETZ	49
FOOTNOTES	49
TYPICAL PERFORMANCE DATA	50
PACKAGE OUTLINE	52
PINOUT:	53
PIN DESCRIPTIONS	54
Power/Ground Pins:	54
Analog Pins:	54
Digital Pins:	55
ORDERING INFORMATION	56

List of Figures

Figure 1: IC Functional BLOCK DIAGRAM.....	5
Figure 2: RTM Output Format.....	9
Figure 3: MPU/CE Communication (Functional).....	10
Figure 4: MPU/CE Communication (Processing Sequence).....	10
Figure 5: SSI Timing, (<i>SSI_FPOL</i> = <i>SSI_RDYPOL</i> = 0).....	19
Figure 6: SSI Timing, 16 bit field example. External device delays SRDY.....	19
Figure 7: Timing relationship between ADC MUX, CE, and Serial Transfers.....	20
Figure 8: Timing Diagram for Voltages, Current and Operation Modes after Power-Up.....	21
Figure 9: Wh Accuracy, 0.3A - 200A/240V.....	50
Figure 10: VARh Accuracy for 0.3A to 200A/240V Performance.....	50
Figure 11: Meter Accuracy over Harmonics at 240V, 30A.....	50
Figure 12: Typical Meter Accuracy over Temperature Relative to 25°C (w/ Temperature Compensation)....	51

List of Tables

Table 1: CE DRAM Locations for ADC Results.....	7
Table 2: Standard Meter Equations.....	8
Table 3: MPU Data Memory Map.....	11
Table 4: External MPU Interrupts.....	12
Table 5: Control Bits for External Interrupts.....	12
Table 6: Timer Modes.....	13
Table 7: Baud Rate Generation.....	15
Table 8: UART Modes.....	15
Table 9: Direction Registers and Internal Resources for DIO Pin Groups.....	16
Table 10: <i>DIO_DIR</i> Control Bit.....	16
Table 11: <i>EECTRL</i> Status Bits.....	17
Table 12: Liquid Crystal Display Segment Table (typical).....	18
Table 13: SSI Pins.....	19
Table 14: Power Saving Measures.....	22

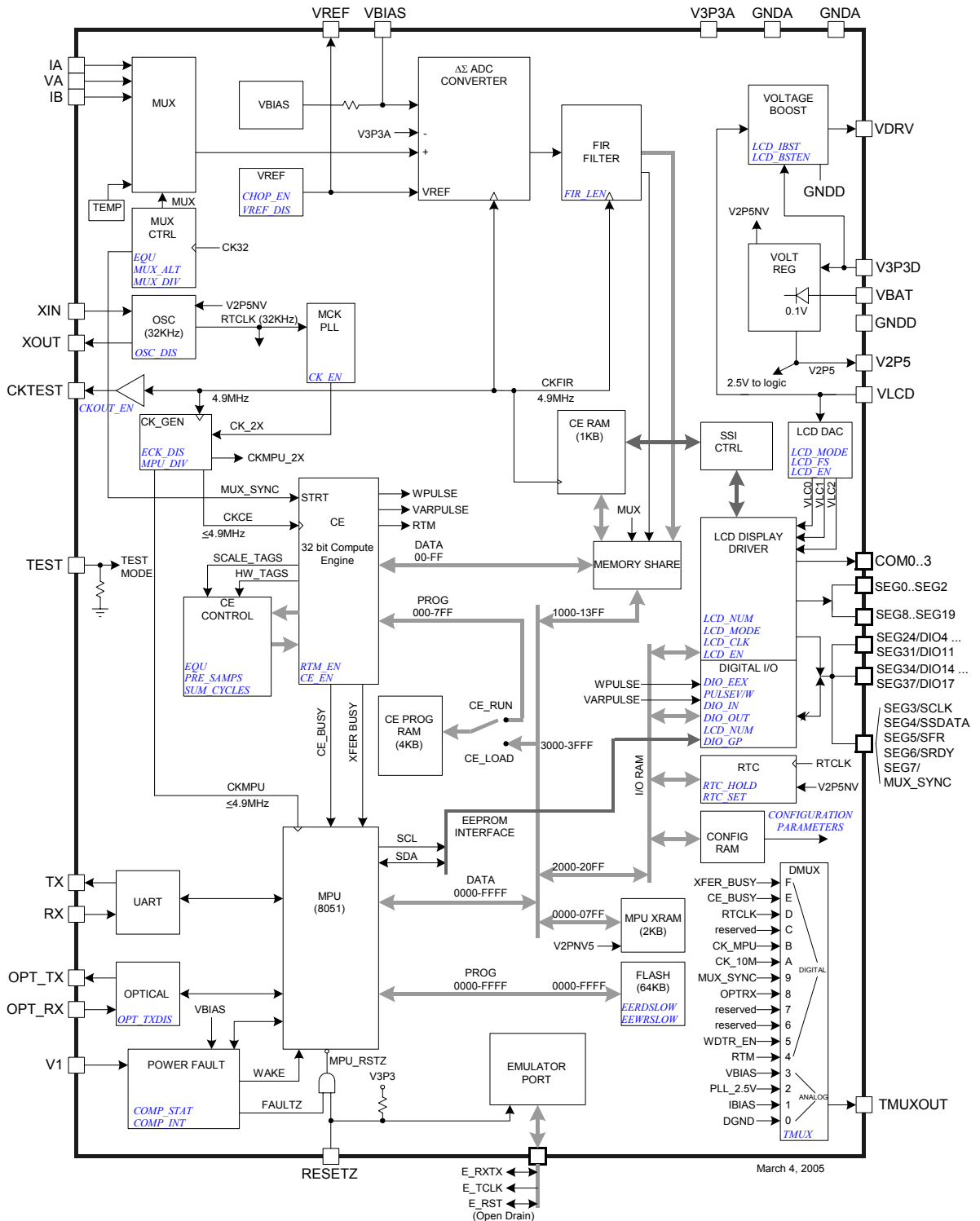


Figure 1: IC Functional BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The TDK 71M6511 single chip power meter integrates all primary functional blocks required to implement a solid-state electricity meter. Included on chip are an analog front end (AFE), an independent digital computation engine (CE), an 8051-compatible microprocessor which executes one instruction per clock cycle (80515), a voltage reference, a temperature sensor, LCD drivers, RAM, Flash memory, a real time clock (RTC), and a variety of I/O pins. Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts, and Rogowski (*di/dt*) Coils.

In a typical application, the 32-bit compute engine (CE) of the 71M6511 sequentially processes the samples from the voltage inputs on pins IA, VA, IB and performs calculations to measure active power (Wh), reactive power (VARh), A²h, and V²h for four quadrant metering. These measurements can then be accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the real time clock function allows the device to record time of use (TOU) metering information for multi-rate applications. Measurements can be displayed on either 3V or 5V LCD commonly used in low temperature environments. Flexible mapping of LCD display segments will facilitate integration if existing custom LCD. Design trade-off between number of LCD segments vs. DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement and RTC accuracy. Temperature dependent external components such as crystal oscillator and current transformers (CT) can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense amplification but it can also function as a standard UART. In addition to the two hardware UART modules, customers can implement a third UART function using a Bit-Bang scheme through two DIO pins. This flexibility makes it possible to implement AMR meters with two ports plus a third Infrared interface. A detailed description of various functions are follows:

Analog Front End (AFE)

The AFE of the 71M6511 is comprised of an input multiplexer, a delta-sigma A/D converter and a voltage reference.

Input multiplexer: The input multiplexer supports up to three input signals that are applied to pins IA, VA and IB of the device. Alternatively, it has the ability to select temperature (TEMP), VA and in some cases, IB. The ALT mux selection is intended to be commanded infrequently (every second or so) by the MPU. In order to prevent disruption of the voltage tracking PLL and voltage allpass networks, VA is not replaced in the ALT selections. Table 2 details the regular and alternative MUX sequences. In some equations, currents must be delayed in allpass networks and therefore cannot be replaced in the ALT selection. Table 2 details the regular and alternative MUX sequences. Missing samples due to an ALT multiplexer sequence are interpolated by the CE.

In a typical application, IA and IB are connected to current transformers that sense the current on each phase of the line voltage. VA is typically connected to voltage sensors through a resistor divider.

MUX Control: MUX advance, FIR filter initiation, and VREF chopping (using the CROSS signal - described below) are controlled by the MUX_CTRL circuit. Additionally, MUX_CTRL launches each pass through the CE program. MUX_CTRL is clocked by CK32, the 32768Hz clock from the PLL block. The behavior of MUX_CTRL is governed by *MUX_ALT*, *EQU*, and *MUX_DIV*.

The *MUX_ALT* bit requests an alternative multiplexer frame. The bit may be asserted on any MPU cycle and may be subsequently de-asserted on any cycle including the next one. A rising edge on *MUX_ALT* will cause MUX_CTRL to wait until the next multiplexer frame and implement a single alternate frame.

Another control input to the multiplexer is *MUX_DIV*. This signal can request 2, 3, 4, or 6 multiplexer states per frame.

Delta-sigma A/D Converter: A single delta-sigma A/D converter digitizes the power inputs to the device. The resolution of the ADC is programmable using the *FIR_LEN* register as shown in the I/O RAM section. ADC resolution can be selected to be 21 bits (*FIR_LEN*=0), or 22 bits (*FIR_LEN*=1). Conversion time is two cycles of CK32 with *FIR_LEN* = 0 and three cycles with *FIR_LEN* = 1. Accuracy and timing specifications in this data sheet are based on *FIR_LEN* = 0.

Initiation of each ADC conversion is controlled by MUX_CTRL as described previously. At the end of each ADC conversion the FIR filter output data is stored into the CE RAM location determined by the multiplexer selection. Table 1 details the RAM locations.

ADDRESS (HEX)	NAME	DESCRIPTION
00	IA	Phase A current
01	VA	Phase A voltage
02	IB	Phase B current
03	-	Reserved
04	-	Reserved
05	-	Reserved
06	TEMP	Temperature
07	--	Reserved

Table 1: CE DRAM Locations for ADC Results

Voltage Reference: The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

Temperature Sensor: Rather than internally compensating for the temperature variation, a digital output corresponding to the bandgap temperature is provided to the embedded MPU, which then digitally compensates the power outputs. This permits a system-wide temperature correction over the entire system than local to the chip. This effective thermal coefficients may include the current sensors, the voltage sensors, and the crystal frequency. Since the band gap is chopper stabilized via the *CHOP_EN* bits, the most significant long-term drift mechanism in the voltage reference is removed.

Digital Computation Engine (CE)

A dedicated 32-bit CE performs the precision computations necessary to accurately measure power. The CE calculations include frequency-insensitive delay cancellation on all six channels (to compensate for the delay between samples caused by the multiplexing scheme) and a frequency insensitive 90° phase shifter for VAR calculations.

Meter Equations: Compute Engine (CE) firmware for industrial configurations implements the equations in Table 2. The register *EQU* (located in the I/O RAM) specifies the equation to be used based on the number of phases used for metering.

<i>EQU</i>	Formula	Channels used from MUX Sequence States 0 → 3				Channels used from alternative MUX Sequence States 0 → 3			
		0	1	2	3	0	1	2	3
000	VA IA (1 element, 2W 1φ)	IA	VA	IB	-	TEMP	VA	-	-
001	VA(IA-IB)/2 (1 element, 3W 1φ)	IA	VA	IB	-	TEMP	VA	IB	-

Table 2: Standard Meter Equations

The number of samples summed is controlled by the bits *PRE_SAMPS* and *SUM_CYCLES* (I/O RAM). The integration time for each energy output is $PRE_SAMPS * SUM_CYCLES / 2520.6$.

Real-Time Monitor: The CE contains a Real-Time Monitor (RTM) which can be programmed through the UART to monitor four selectable CE RAM locations at full sample rate. The four monitored locations are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass. The RTM can be enabled and disabled with *RTM_EN*. The RTM output is clocked by CKTEST. Each RTM word is clocked out in 35 cycles and contains a leading flag bit. Figure 1 illustrates the RTM output format. RTM is low when not in use

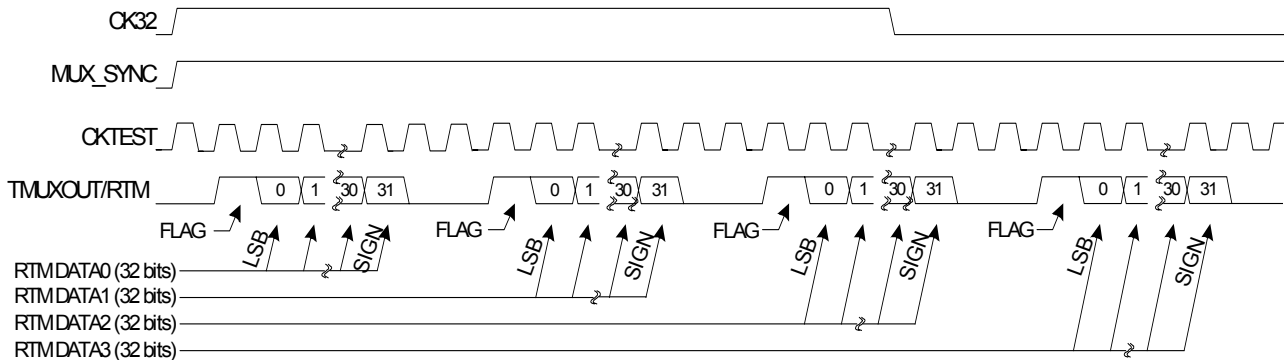


Figure 2: RTM Output Format

Clock Generator: The CE clock frequency is always $CK32 * 150$. The MPU clock frequency is determined by MPU_DIV and can be $CE * 2^{-MPU_DIV}$ Hz where MPU_DIV varies from 0 to 7 (MPU_DIV is 0 on power-up). This makes the MPU clock scalable from 4.9152MHz down to 38.4kHz. CK32 is the 32kHz clock. The circuit also generates a 2x MPU clock for use by the emulator. This clock is not generated when ECK_DIS is asserted by the MPU.

CE RAM: The CE data RAM can be accessed by the FIR filter block, the RTM, the CE, and the MPU. Assigned time slots are reserved for FIR, RTM, and MPU, respectively, such that memory accesses to CE RAM do not collide. Holding registers are used to convert 8-bit wide MPU data to/from 32-bit wide CE RAM data, and wait states are inserted as needed, depending on the frequency of CKMPU. RTM data is read from the CE RAM locations specified by $RTM0$, $RTM1$, $RTM2$, and $RTM3$ after the rise of MUX_SYNC .

CE PRAM: The CE program RAM is loaded at boot time by the MPU and then accessed as necessary by the CE. Each CE instruction word is 2 bytes long. PRAM memory size is 2048 words. The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the MUX_SYNC signal rises.

CE Communication with MPU: Figure 3 shows the functional relationship between CE and MPU. The CE is controlled by the MPU via shared registers in the I/O RAM and by registers in the CE RAM. The CE outputs two interrupt signals to the MPU: CE_BUSY and $XFER_BUSY$, which are connected to the MPU interrupt service inputs. CE_BUSY indicates that the CE is actively processing data. This signal will occur once every multiplexer frame. $XFER_BUSY$ indicates that the CE is updating data to the output region of the CE RAM. This will occur whenever the CE has finished generating a sum, completing a cycle determined by $SUM_CYCLES * PRE_SAMPs$ samples. Interrupts to the MPU occur on the falling edges of these signals.

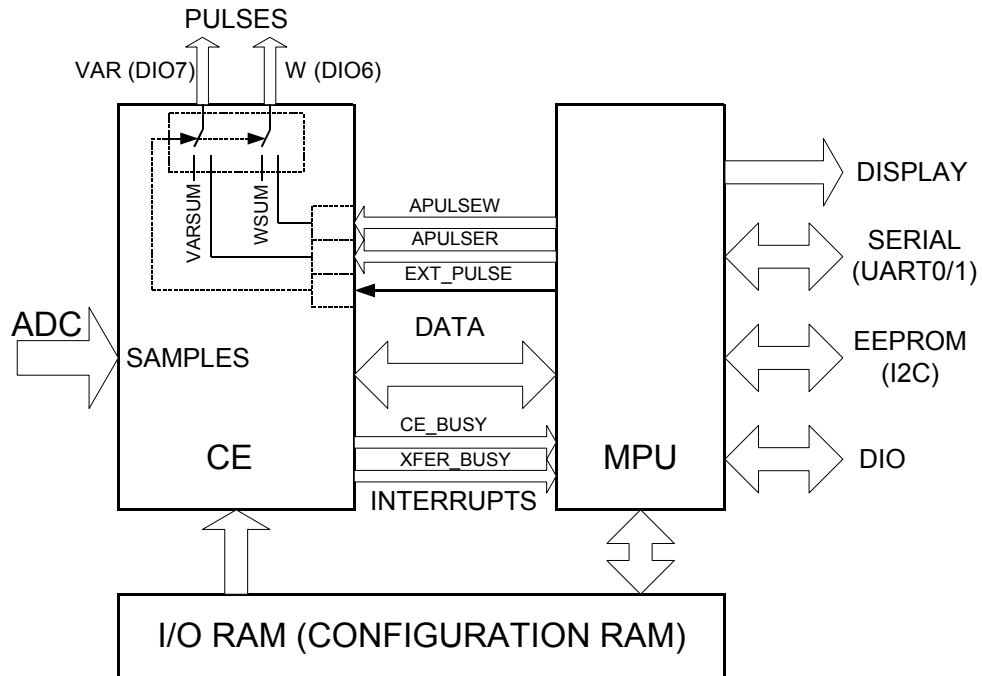


Figure 3: MPU/CE Communication (Functional)

Figure 4 shows the sequence of events between CE and MPU. In a typical application, the MPU loads the code for the CE into the CE PRAM and CE constants into the CE DRAM upon power-up. It then starts the CE by setting the *CE_EN* bit. The CE then repetitively executes its code, generating results and storing them in the CE RAM. The MPU will wait for the CE to signal that fresh data is ready (the XFER interrupt). It will read the data and perform additional processing such as energy accumulation.

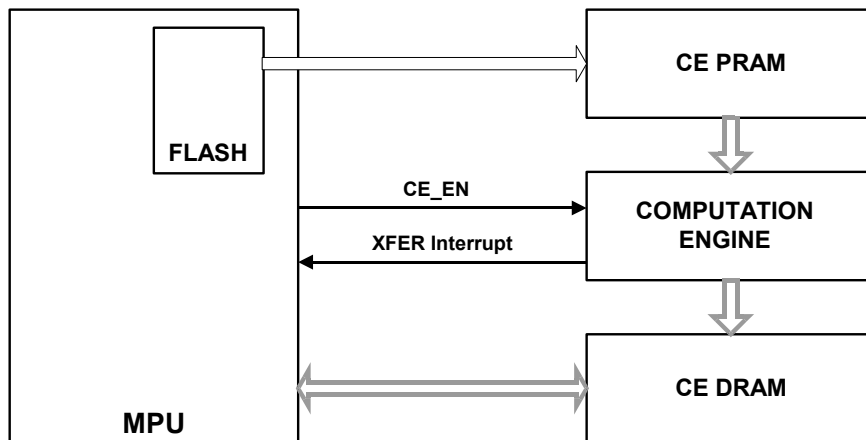


Figure 4: MPU/CE Communication (Processing Sequence)

Pulse Generator: The chip contains two pulse generators which create low jitter pulses at a rate set by $APULSEW*WRATE$ and $APULSER*WRATE$ if EXT_PULSE (a CE input variable in CE DRAM) is 15. If EXT_PULSE is 0 $APULSEW$ is replaced with $WSUM_X$ and $APULSER$ is replaced with $VARSUM_X$ (see Figure 3). The DIO_PV and DIO_PW bits as described in the Digital I/O section can be programmed to route WPULSE and VARPULSE to the output pins DIO7 and DIO6 respectively.

80515 MPU Core

The device includes an 80515 MPU (8-bit, 8051-compatible) that processes one instruction each clock cycle. Using a 5MHz clock results in a processing throughput of 5 MIPS. Actual processor clocking speed can be adjusted to the total processing demand of metering calculations, AMR management, memory management, LCD driver management and I/O management.

Typical measurement and metering functions based on the results provided by the internal 32-bit compute engine (CE) are available for the MPU as part of TDK's standard library. A standard ANSI "C" 80515 application programming interface library is available to help reduce design cycle.

The MPU core has addressable memory space of up to 64k-bytes. Data bus address space is allocated to on-chip memory as shown in Table 3.

Address (hex)	Memory Technology	Memory Type	Typical Usage	Wait States (at 5MHz)	Memory Size (bytes)
0000-FFFF	Flash Memory	Non-volatile	Program and non-volatile data	0	64KB
0000-07FF	Static RAM	Battery-buffered	MPU data XRAM,	0	2KB
1000-13FF	Static RAM	Volatile	CE data	5	1KB
2000-20FF	Static RAM (in 80515 core)	Volatile	Miscellaneous I/O RAM (configuration RAM)	0	256
3000-3FFF	Static RAM	Volatile	CE Program code	5	4KB

Table 3: MPU Data Memory Map

Interrupts: The 71M6511 MPU allows seven external interrupts. These are connected as shown in table 5. The direction of interrupts 2 and 3 is programmable in the MPU. Interrupts 2 and 3 should be programmed for falling sensitivity. The generic 8051 MPU literature states that interrupt 4 through 6 are defined as rising edge sensitive. Thus, the hardware signals attached to interrupts 5 and 6 are inverted to achieve the edge polarity shown in Table 4.

External Interrupt	Connection	Polarity	Flag Reset
0	Digital I/O High Priority	see <i>DIO_Rx</i>	automatic
1	Digital I/O Low Priority	see <i>DIO_Rx</i>	automatic
2	Comparator	falling	automatic
3	CE_BUSY	falling	automatic
4	Comparator	rising	automatic
5	EEPROM busy	falling	automatic
6	XFER_BUSY OR RTC_1SEC	falling	manual

Table 4: External MPU Interrupts

Enable Bit	Description	Flag Bit	Description
EX0	Enable external interrupt 0	IE0	External interrupt 0 flag
EX1	Enable external interrupt 1	IE1	External interrupt 1 flag
EX2	Enable external interrupt 2	IEX2	External interrupt 2 flag
EX3	Enable external interrupt 3	IEX3	External interrupt 3 flag
EX4	Enable external interrupt 4	IEX4	External interrupt 4 flag
EX5	Enable external interrupt 5	IEX5	External interrupt 5 flag
EX6	Enable external interrupt 6	IEX6	External interrupt 6 flag
<i>EX_XFER</i>	Enable XFER_BUSY interrupt	<i>IE_XFER</i>	XFER_BUSY interrupt flag
<i>EX_RTC</i>	Enable RTC_1SEC interrupt	<i>IE_RTC</i>	RTC_1SEC interrupt flag

Table 5: Control Bits for External Interrupts

SFR (special function register) enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit which is set by the interrupt hardware and is reset automatically by the MPU interrupt handler (0 through 5). XFER_BUSY and RTC_1SEC, which are OR-ed together, have their own enable and flag bits in addition to the interrupt 6 enable and flag bits (see Table 5), and these interrupts must be cleared by the MPU software.

Internal Resources

Oscillator: The oscillator drives a standard 32.768kHz watch crystal. Crystals of this type are accurate and do not require a high current oscillator circuit. The oscillator in the TDK 71M6511 Power Meter IC has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to the VBAT pin.

PLL: All internal clocks are based on the watch crystal frequency (32,768Hz). The PLL multiplies this frequency by 150 to yield 4.9152MHz. This frequency is supplied to the ADC, which then supplies the clock to the FIR filter (CKFIR), the clock test output pin (CKTEST), the CE RAM and the clock generator. The clock generator provides two clocks, one for the MPU (CKMPU) and one for the CE (CKCE).

Clock/Timers: Timing for the device is derived from the 32.768kHz watch crystal. On-chip timing functions include the 80515 master clock, a real time clock (RTC), delta-sigma sample clock, and two 80515 general counter/timers, timer 0 and timer 1.

Table 6 specifies the combinations of operation modes allowed for timer 0 and timer 1:

	Timer 1		
	Mode 0	Mode 1	Mode 2
Timer 0 - mode 0	YES	YES	YES
Timer 0 - mode 1	YES	YES	YES
Timer 0 - mode 2	Not allowed	Not allowed	YES

Table 6: Timer Modes

Real-Time Clock (RTC): The RTC is driven directly by the crystal oscillator. It is powered by the V2P5NV net, which is the battery-backed up supply. The RTC consists of a counter chain and output registers. The counter chain consists of seconds, minutes, hours, day of week, day of month, month, and year. The RTC is capable of processing leap years. Each counter has its own output register. Whenever the MPU reads the seconds register, all other output registers are automatically updated. Since the RTC clock is not coherent to the MPU clock, the MPU must read the seconds register until two consecutive reads are the same (requires either 2 or 3 reads). At this point, all RTC output registers will have the correct time. Regardless of the MPU clock speed, RTC reads require 1 wait state.

RTC time is set by writing to the registers. Each byte written to RTC must be delayed at least 3 RTC cycles from any previous byte written to RTC.

Two time correction bits, *RTC_DEC_SEC* and *RTC_INC_SEC* are provided to adjust the RTC time. A pulse on one of these bits causes the time to be decremented or incremented by an additional second at the next update of the *RTC_SEC* register. Thus, if the crystal temperature coefficient is known, the MPU firmware can integrate temperature and correct the RTC time as necessary as discussed in temperature compensation.

Temperature Sensor: The device includes an on-chip temperature sensor for determining the temperature of the bandgap reference. The MPU may request an alternate multiplexer frame containing the temperature sensor output by asserting *MUX_ALT*. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see section titled "Temperature Compensation").

The secondary use of the temperature data is to monitor the ambient temperature of the meter. In a typical application, the temperature of the 71M6511 compared to the ambient temperature within the meter is characterized. Based on this characterization data, an over-temperature value can be determined. The on-chip temperature can also be monitored to determine if the ambient is approaching an unsafe level. In the event that the temperature exceeds the set level, certain I/O functions that disable power supplies, contact the utility through an AMR port, measure the duration of the over-temp condition, etc., can be initiated under firmware control.

Memory

Flash Memory: The 71M6511 includes 64KB of on-chip flash memory. The flash memory is intended to primarily contain MPU program code. In a typical application, it also contains images of the CE program code, CE coefficients, MPU RAM, and I/O RAM. On power-up, before enabling the CE, the MPU must copy these images to their respective memory locations.

The bit *FLASH66Z* (see I/O RAM table) defines the speed for accessing flash memory. To minimize supply current draw, this bit should be set to 1.

Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

The mass erase sequence is:

1. Write 1 to the *FLSH_MEEN* bit (SFR address 0xB2[1]).
2. Write pattern 0xAA to *FLSH_ERASE* (SFR address 0x94)

Note: The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to *FLSH_PGADR* (SFR address 0xB7[7:1])
2. Write pattern 0x55 to *FLSH_ERASE* (SFR address 0x94)

The MPU may write to the flash memory. This is one of the non-volatile storage options available to the user. The other option, battery backed-up RAM, is the lower supply current option for non-volatile storage.

FLSH_PWE (flash program write enable) differentiates 80515 data store instructions (*MOVX@DPTR,A*) between Flash and XRAM writes.

MPU RAM: The 71M6511 includes 2k-bytes of static RAM memory on-chip (XRAM) which are backed-up by the battery plus 256-bytes of internal RAM in the MPU core. The 2k-bytes of static RAM are used for data storage during normal MPU operations.

CE RAM: The CE RAM is the working memory of the CE, for both program (CE PRAM) and data (CE DRAM). The MPU can read and write the CE RAM as the primary means of data communication between the two processors. CE PRAM cannot be accessed by the MPU when the CE is running.

I/O Peripherals

The 71M6511 includes several I/O peripheral functions that improve the functionality of the device and reduce the component count for most meter applications. The I/O peripherals include two UARTs, digital I/O, comparator inputs, LCD display drivers, I²C interface and an IR interface.

Note: Clock stretching and multi-master operation is not supported for the I²C interface.

UART Interface: The 71M6511 includes a UART that can be programmed to communicate with a variety of AMR modules. Under MPU control, the UART can also provide a mechanism for programming the on-chip flash memory. A second UART is connected to the optical port, as described in the optical port description.

The UART is a dedicated 2-wire serial interface, which can communicate with an external host processor at up to 38,400 bits/s (with MPU clock = 1.2288MHz). The operation of each pin is as follows:

RX: Is the serial input data. Conforming to RS-232 standard, the bytes are input LSB first.

TX: Is the serial output data. The bytes are output LSB first.

The 71M6511 has several on-chip registers which can be read and written. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 38400 bps. Table 7 shows how the baud rates are calculated. Table 8 shows the selectable UART operation modes.

	Using Timer 1	Using Internal Baud Rate Generator
Serial Interface 0	$2^{\text{smod}} * f_{\text{CKMPU}} / (384 * (256 - \text{th1}))$ th1= high byte of timer 1	$2^{\text{smod}} * f_{\text{CKMPU}} / (64 * (2^{10} - \text{s0rel}))$
Serial Interface 1	N/A	$f_{\text{CKMPU}} / (32 * (2^{10} - \text{s1rel}))$

Note: s0rel and s1rel are 10 bit values derived by combining bits from the respective timer reload registers. smod is the smod bit in the special function register pcon.

Table 7: Baud Rate Generation

	UART 0	UART 1
Mode 0	N/A	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator)
Mode 1	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1)	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator)
Mode 2	Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of f_{CKMPU}	N/A
Mode 3	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1)	N/A

Table 8: UART Modes

Optical Interface

The device includes an interface to implement an IR or optical port. The pin OPT_Tx is designed to directly drive an external LED for transmitting data on an optical link (low-active). The pin OPT_Rx, also low-active, is designed to sense the input from an external photo detector used as the receiver for the optical link. These two pins are connected to a dedicated UART port. OPT_Tx can be tristated if it is desired to multiplex another IO pin to the OPT_Tx output, e.g. for combined use of the same LED by the OPT_TX pin and by a DIO pin implementing a pulse generator. The control bit is *OPT_TXDIS*.

Digital I/O

The device includes up to 12 pins of general purpose digital I/O. These pins are dual function and can alternatively be used as LCD drivers. The pins are configured by the *DIO* registers and by the five bits of the *LCD_NUM* register (located in I/O RAM). Each pin can be configured independently as an input or output with the *DIO_DIRn* bits. A 3-bit configuration word, *DIO_Rx*, can be used for certain pins, when configured as inputs, to individually assign an internal resource such as an interrupt or a timer control. Table 9 lists the direction registers and configurability associated with each group of DIO pins. Table 10 shows the configuration for a DIO pin through its associated bit in its *DIO_DIR* register.

DIO Pin Group	Type	Direction Register Name	Direction Register Location	Internal resources selectable when configured as input
DIO_0...DIO_3	DIO only	<i>DIO_DIR0</i>	SFR A2 [3:0]	Yes
DIO4...DIO7	Multi-use	<i>DIO_DIR0</i>	SFR A2 [7:4]	Yes
DIO8...DIO11	Multi-use	<i>DIO_DIR1</i>	SFR 91 [3:0]	Yes
DIO12...DIO15	Multi-use	<i>DIO_DIR1</i>	SFR 91 [7:4]	No
DIO16...DIO21	Multi-use	<i>DIO_DIR2</i>	SFR A1 [5:0]	No

Table 9: Direction Registers and Internal Resources for DIO Pin Groups

	<i>DIO_DIR [n]</i>	
	0	1
DIO Pin n Function	input	output

Table 10: *DIO_DIR* Control Bit

Additionally, if DIO6 and DIO7 are declared outputs, they can be configured as dedicated pulse outputs (WPULSE = DIO6, VARPULSE = DIO7) using *DIO_PW* and *DIO_PV* registers. In this case, DIO6 and DIO7 are under CE control. DIO4 and DIO5 can be configured to implement the EEPROM Interface.

Analog and Digital Output Multiplexer:

One out of 12 digital or 4 analog signals can be selected to be output on the TMUXOUT pin. The function of the multiplexer is controlled with the *TMUX* bits (located in the I/O RAM).

EEPROM Interface

A dedicated 2-pin serial interface communicates with external EEPROM devices. The interface is multiplexed onto DIO4 (SCK) and DIO5 (SDA). See *DIO_EEX* bit in the I/O RAM table. The MPU communicates with the interface through two SFR registers: *EEDATA* and *EECTRL*. If the MPU wishes to write a byte of data to EEPROM, it places the data in *EEDATA* and then writes the 'Transmit' code to *EECTRL*. The write to *EECTRL* initiates the transmit. The transmit is finished when the Busy bit falls. INT5 is also asserted when BUSY falls. The MPU can then check the *RX_ACK* bit to see if the EEPROM acknowledged the transmission.

A byte is read by writing the 'Receive' command to *EECTRL* and waiting for Busy to fall. Upon completion, the received data is in *EEDATA*. The serial transmit and receive clock is 78kHz during each transmission, and then holds in a high state until the next transmission. The bits in *EECTRL* are shown in Table 11.

The EEPROM interface can also be operated by controlling the DIO4 and DIO5 pins directly.

Status Bit	Name	Read/Write	Polarity	Description																
7	<i>Error</i>	R	High	Asserted when an illegal command is received.																
6	<i>Busy</i>	R	High	Asserted when serial data bus is busy.																
5	<i>RX_ACK</i>	R	High	Indicates the EEPROM sent an ACK bit.																
4	<i>TX_ACK</i>	R	High	Indicates when an ACK bit has been sent to EEPROM																
3-0	<i>CMD[3:0]</i>	W	See CMD Table	<table border="1"> <thead> <tr> <th>CMD</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No-op</td> </tr> <tr> <td>2</td> <td>Receive a byte from EEPROM and send ACK.</td> </tr> <tr> <td>3</td> <td>Transmit a byte to EEPROM</td> </tr> <tr> <td>5</td> <td>Issue a 'STOP' sequence</td> </tr> <tr> <td>6</td> <td>Receive the last byte from EEPROM and don't send ACK.</td> </tr> <tr> <td>9</td> <td>Issue a 'START' sequence</td> </tr> <tr> <td>Others</td> <td>No Operation, assert Error bit</td> </tr> </tbody> </table>	CMD	Operation	0	No-op	2	Receive a byte from EEPROM and send ACK.	3	Transmit a byte to EEPROM	5	Issue a 'STOP' sequence	6	Receive the last byte from EEPROM and don't send ACK.	9	Issue a 'START' sequence	Others	No Operation, assert Error bit
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				5	Issue a 'STOP' sequence															
				6	Receive the last byte from EEPROM and don't send ACK.															
9	Issue a 'START' sequence																			
Others	No Operation, assert Error bit																			

Table 11: *EECTRL* Status Bits

LCD Drivers

The device contains 19 dedicated LCD segment drivers and 17 multi-purpose pins which may be configured as additional LCD segment drivers. The device is capable of driving between 60 to 128 pixels of LCD display with 25% duty cycle. At 7 pixels per digit, the LCD can be designed for 8 to 18 digits of display. Since each pixel is addressed individually, the LCD display can be a combination of alphanumeric digits and enunciator symbols (see Table 13). The LCD drivers are grouped into 4 commons (COM0 to COM3) and up to 32 segments. A typical LCD map is shown below. A charge pump suitable for driving VLCD is included. This circuit creates 5V from the 3.3V supply. A contrast DAC is provided that permits the LCD full scale to be adjusted between VLCD and 70% of VLCD. *LCD_NUM* defines the number of dual purpose pins used for LCD segment interface.

	Seg0	Seg1	Seg2	Seg3	Seg4	Seg5	Seg31
Com0	P0	P4	P8	P12	P16	P20	P124
Com1	P1	P5	P9	P13	P17	P21	P125
Com2	P2	P6	P10	P14	P18	P22	P126
Com3	P3	P7	P11	P15	P19	P23	P127

Table 12: Liquid Crystal Display Segment Table (typical)

Note: P0, P1, ... Represent the pixel numbers on the LCD.

Synchronous Serial Interface (SSI)

A high-speed serial interface with handshake capability is available to send a contiguous block of CE data to an external data logger or DSP. The block of data, configurable as to location and size, is sent starting 1 cycle of 32kHz before each CE code pass begins. If the block of data is big enough that transmission has not completed when the code pass begins, it will complete during the CE code pass with no timing impact to the CE or the serial data. In this case, care must be taken that the transmitted data is not modified unexpectedly by the CE. The SSI interface is enabled by the *SSI_EN* bit and consists of SCLK, SSDATA, and SFR as outputs and, optionally, SRDY as input. The interface is compatible with 16-bit and 32-bit processors. The operation of each pin is as follows:

SCLK is the serial clock. The clock can be 5MHz or 10MHz, as specified by the *SSI_10M* bit. The *SSI_CKGATE* bit controls whether SCLK runs continuously or is gated off when no SSI activity is occurring. If SCLK is gated, it will begin 3 cycles before SFR rises and will persist 3 cycles after the last data bit is output.

SSDATA is the serial output data. SSDATA changes on the rising edge of SCLK and outputs the contents of a block of CE RAM words starting with address *SSI_STRT* and ending with *SSI_END*. The words are output MSB first.

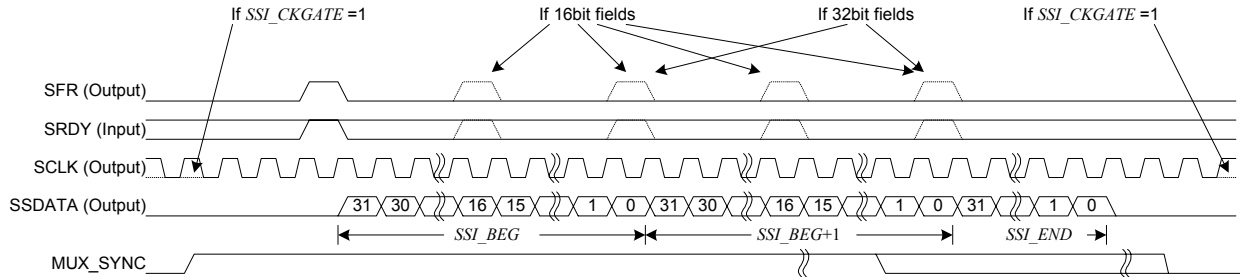


Figure 5: SSI Timing, (SSI_FPOL = SSI_RDYPOL = 0)

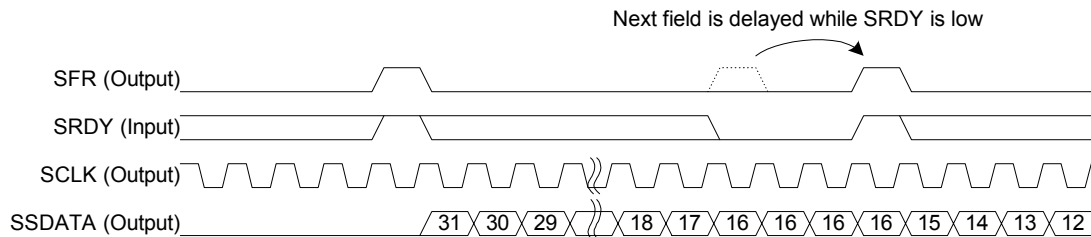


Figure 6: SSI Timing, 16 bit field example. External device delays SRDY.

SFR is the framing pulse. Although CE words are always 32 bits, the SSI interface will frame the entire data block as a single field, as multiple 16 bit fields, or as multiple 32-bit fields. The SFR pulse is one clock cycle wide, changes state on the rising edge of SCLK and precedes the first bit of each field. The field size is set with the *SSI_FSIZE* register: 0 entire data block, 1-8 bit fields, 2-16 bit fields, 3-32 bit fields. The polarity of the SFR pulse can be inverted with *SSI_FPOL*. If SRDY does not delay it, the first SFR pulse in a frame will rise on the third SCLK after MUX_SYNC (fourth SCLK if 10MHz). MUX_SYNC can be used to synchronize the fields arriving at the data logger or DSP. When using the SSI interface, the *LCD_EN* flag in DIO RAM should be disabled in order to obtain undisturbed SSI signals.

The pins used for the SSI are multiplexed with the LCD segment outputs, as shown in table 13.

SSI SIGNAL	LCD SEGMENT OUTPUT PIN
SCLK	SEG3
SSDATA	SEG4
SFR	SEG5
SRDY	SEG6

Table 13: SSI Pins

SRDY is an optional handshake input that indicates that the DSP or data logging device is ready to receive data. SRDY must be high to enable SFR to rise and initiate the transfer of the next field. It is expected that SRDY changes state on the rising edges of SCLK. If SRDY is not high when the SSI port is ready to transmit the next

field, transmission will be delayed until it is. SRDY is ignored except at the beginning of a field transmission. If SRDY is not enabled (by *SSI_RDYEN*), the SSI port will behave as if SRDY is always one.

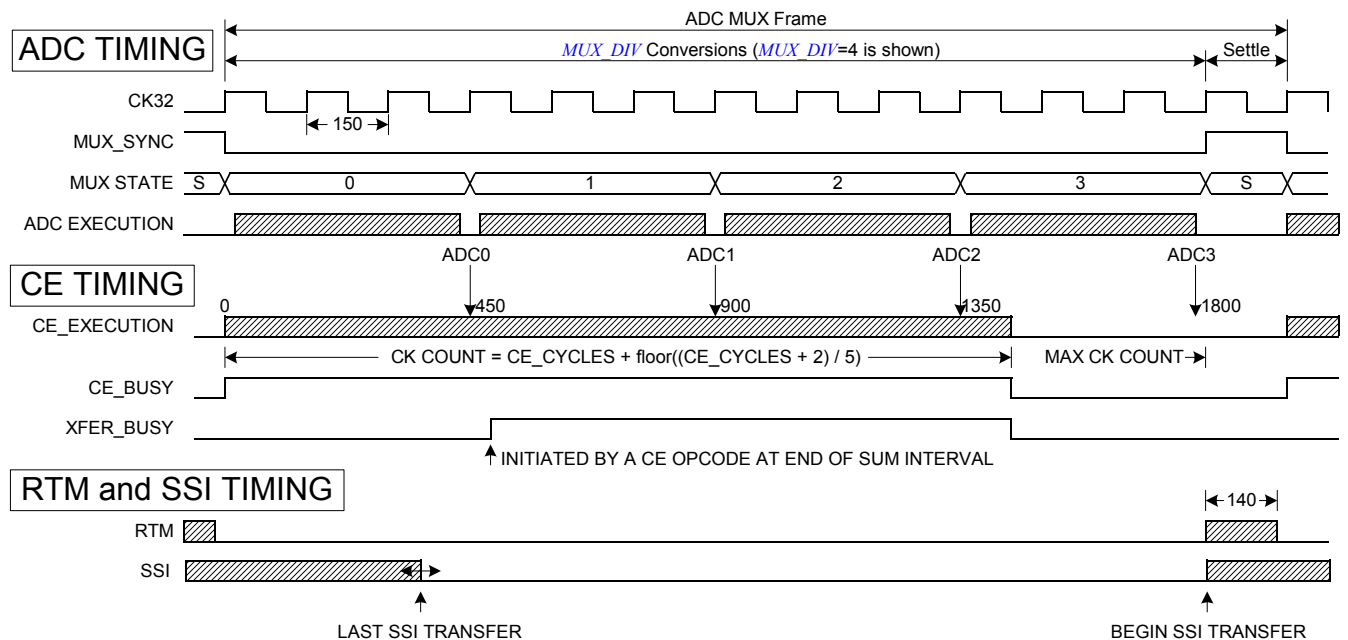
System Timing Summary

Figure 7 summarizes the timing relationships between the input multiplexer states, the CE_BUSY signal, and the two serial output streams. In this example, *MUX_DIV* = 1 (four mux states) and *FIR_LEN* = 1 (3 CK32 cycles). Since FIR filter conversions require two or three CK32 cycles, the duration of each MUX frame is 1 + 2 * states defined by *MUX_DIV* if *FIR_LEN* = 0, and 1 + 3 * states defined by *MUX_DIV* if *FIR_LEN* = 1. Followed by the conversions is a single CK32 cycle.

Each CE program pass begins when MUX_SYNC falls. Depending on the length of the CE program, it may continue running until the end of the ADC3 conversion. CE opcodes are constructed to ensure that all CE code passes consume exactly the same number of cycles. The result of each ADC conversion is inserted into the CE DRAM when the conversion is complete. The CE code must be written to tolerate sudden changes in ADC data. The exact CK count when each ADC value is loaded into DRAM is shown in Figure 7.

Figure 7 also shows that the serial RTM data stream, begin transmitting at the beginning of MUX_SYNC. RTM, consisting of 140 CK cycles, will always finish before the next code pass starts. The SSI port begins transmitting at the same time as RTM, but may significantly overrun the next code pass if a large block of data is required. Neither the CE nor the SSI port will be affected by this overlap.

ADC, CE and SERIAL TIMING



- NOTES:
1. ALL DIMENSIONS ARE 5MHZ CK COUNTS.
 2. THE PRECISE FREQUENCY OF CK IS 150*CRYSTAL FREQUENCY = 4.9152MHz.
 3. XFER_BUSY OCCURS ONCE EVERY (PRESAMPS * SUM_CYCLES) CODE PASSES.

Figure 7: Timing relationship between ADC MUX, CE, and Serial Transfers.

Fault and Reset Behavior

Reset Mode: When the RESETZ pin is pulled low or when $V1 < VBIAS$, all digital activity in the chip stops while analog circuits are still active. The oscillator and RTC module continue to run. Additionally, all I/O RAM bits are cleared. As long as $V1$, the input voltage at the power fault block, is greater than $VBIAS$, the internal 2.5V regulator will continue to provide power to the digital section.

Once initiated, the reset mode will persist until the reset timer times out, signified by WAKE rising. This will occur in 4100 cycles of the real time clock after RESETZ goes high, at which time the MPU will begin executing its pre-boot and boot sequences from address 00. See the security section for more description of preboot and boot.

Power Fault Circuit: The $V1$ input is connected to the power fault detection circuitry. The output of power fault detection circuit controls WAKE and FAULTZ signals. Upon power fault, WAKE and FAULTZ are both lowered immediately to stop the MPU and engage the battery backup circuit for RTC and MPU DRAM. When power fault ends, FAULTZ rises immediately and disengages the battery backup. The MPU remains in reset and will not start until 4100 OSC clocks later, when WAKE rises. The delay before asserting WAKE permits the MCK PLL to settle.

Power-Up: After power-up, the device is in reset as long as $V1 < VBIAS$. As soon as $V1$ exceeds $VBIAS$, the reset timer is started which takes the device out of reset after 4100 oscillator cycles (see Figure 8). The MPU then initiates its pre-boot phase lasting 32 cycles. The supply current will be low but not zero during power-up. It will increase, once $V1$ exceeds $VBIAS$ and will increase to the nominal value once the preboot phase starts. The supply current may then be reduced under firmware control, following the steps specified in Battery Operation and Power Save Modes.

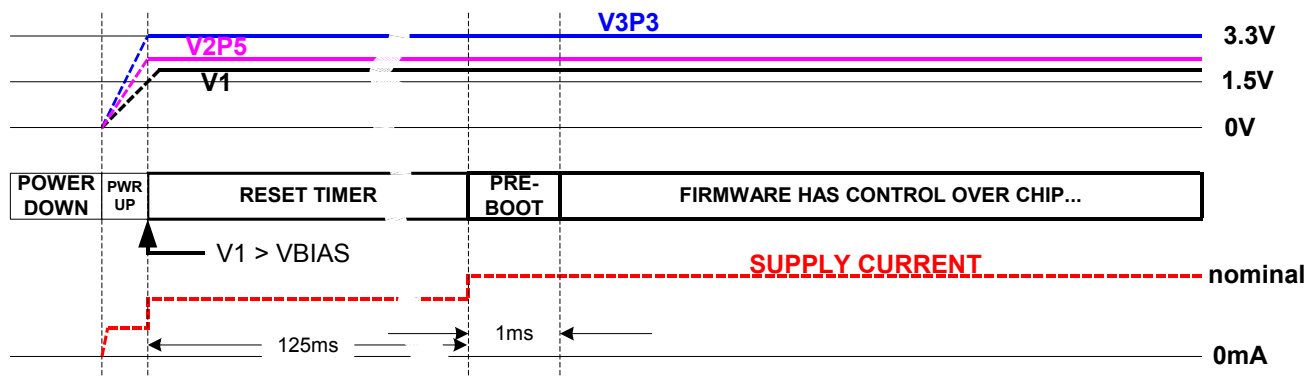


Figure 8: Timing Diagram for Voltages, Current and Operation Modes after Power-Up

Battery Operation/Power Save Modes

When $V1$ is lower than $VBIAS$, the external battery will power the following parts of the 71M6511 via the V2P5NV internal voltage net:

- RTC
- Crystal oscillator circuitry
- MPU XRAM
- WD_OVF bit

In normal mode of operation, running on 3.3V supply, various resources of the device may be shut down by the MPU firmware in order to reduce power consumption while other essential resources such as UARTs may remain active. Table 14 outlines these resources and their typical current consumption (based on initial condition $MPU_DIV = 0$).

Power Saving Measure	Software Control	Typical Savings
Disable the CE	$CE_EN = 0$	0.16mA
Disable the ADC	$ADC_DIS = 1$	1.8mA
Disable clock test output CKTEST	$CKOUTDIS = 1$	0.6mA
Disable emulator clock	$ECK_DIS = 1$	0.1mA
Set flash read pulse timing to 33 ns	$FLASH66Z = 1$	0.04mA
Disable the LCD voltage boost circuitry	$LCD_BSTEN = 0$	0.9mA
Disable RTM outputs	$RTM_EN = 0$	0.01mA
Reduce the clock for the MPU	$MPU_DIV = 5$	0.4mA

Table 14: Power Saving Measures

Watchdog Timer

In addition to the basic watchdog timer included in the 80515, an independent, robust, fixed duration, watchdog timer (WD) is included in the device. It uses the RTC crystal oscillator as its timebase and requires a firmware reset at least every 1.5 seconds. When the WDT overflow occurs, the part is momentarily reset as if RESETZ were pulled low for half of a crystal oscillator cycle. Thus, 4100 cycles later, the MPU will be launched from address 00.

A status bit, WD_OVF , is set when WDT overflow occurs. This bit is powered by the NV supply and can be read by the MPU when WAKE rises to determine if the part is initializing after a WD overflow event or after a power up. After it is read, MPU firmware must clear WD_OVF . The WD_OVF bit is cleared by the RESETZ pin

The watchdog timer also includes an oscillator check. If the crystal oscillator stops or slows down, WD_OVF is set and a system reset will be performed when the crystal oscillator resumes.

There is no internal digital state that deactivates the WDT. For debug purposes, however, the WD can be disabled by tying the V1 pin to V3P3. Of course, this also deactivates V1 power fault detection. Since there is no firmware way to disable the crystal oscillator or the WD, it is guaranteed that whatever state the part might find itself in, upon watchdog overflow, the part will be reset to a known state.

In normal operation, the WD is reset by periodically writing a one to the WDT_RST bit. The watchdog timer is also reset when WAKE=0 and, during development, when a 14h command is received from the ICE.

Program Security

When enabled, the security feature limits the ICE to global flash erase operations only. All other ICE operations are blocked. This guarantees the security of the user's MPU and CE program code. Security is enabled by MPU code that is executed in a 32 cycle preboot interval before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the flash, followed by a chip reset. Global flash erase also clears the CE program RAM.

The first 32 cycles of the MPU boot code are called the preboot phase because during this phase the ICE is inhibited. A read-only status bit, *PREBOOT*, identifies these cycles to the MPU. Upon completion of preboot, the ICE can be enabled and is permitted to take control of the MPU.

SECURE, the security enable bit, is reset whenever the chip is reset. Hardware associated with the bit permits only ones to be written to it. Thus, preboot code may set *SECURE* to enable the security feature but may not reset it. Once *SECURE* is set, the preboot code is protected and no external read of program code is possible

Specifically, when *SECURE* is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's preboot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase. Note that global flash erase erases CE program RAM whether *SECURE* is set or not.
- Writes to page zero, whether by MPU or ICE are inhibited.

Voltage Reference

Initial Calibration: The internal voltage reference is calibrated during device manufacture. Trim data is stored in on-chip fuses and is not accessible to the user.

Temperature Compensation: The internal voltage reference has a predictable temperature dependency that, if not compensated, can result in measurement errors.

For the 71M6511, the temperature coefficients TC1 and TC2 are given as constants that represent typical component behavior.

For the 71M6511H, the temperature characteristics of the chip are measured during production and then stored in the fuse registers *TRIMBGA*, *TRIMBGB* and *TRIMM[2:0]*. TC1 and TC2 can be derived from the fuses by using the relations given in the Electrical Specifications section.

TRIMM[2:0], *TRIMBGA* and *TRIMBGB* are read by first writing either 4, 5 or 6 to *TRIMSEL* (20FD) and then reading the value of *TRIM* (20FF).

The MPU can use the information from the fuse registers to compensate for temperature variation of the reference, along with other system components such as the crystal and the input attenuators, by reading the temperature output of the CE and modifying the gain constants accordingly.

Application Information

Meter Calibration: Once the TDK 71M6511 power meter device has been installed in a meter system, it has to be calibrated for tolerances of the current sensors, voltage dividers and signal conditioning components. The device can be calibrated using the gain and phase adjustment factors accessible to the CE. The gain adjustment is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. Phase adjustment is provided to compensate for phase shifts introduced by the current sensors.

Due to the flexibility of the MPU firmware, any calibration method, such as calibration based on energy, or current and voltage, segment-wise calibration (depending on current range) can be implemented.

Temperature Compensation for the RTC: The flexibility provided by the MPU allows for compensation of the RTC depending on substrate temperature.

MPU Firmware Library: All application-specific MPU functions mentioned above under “Application Information” are available from TDK as a standard ANSI C library. This library is available as part of the Demonstration Kit for the 71M6511 and 71M6511H ICs. The Demonstration Kits come with the 71M6511 or 71M6511H IC pre-programmed with demo firmware mounted on a functional sample meter PCB (Demo Board). The Demo Boards allow for quick and efficient evaluation of the IC without having to write firmware or having to supply an in-circuit emulator (ICE).

A reference guide for firmware development on the 71M6511 and 71M6511H is available as a separate document (Software User’s Guide). The User’s Manuals supplied with the Demo Kits contain MPU address maps for the demo code as well as other useful information, such as sample calibration procedures.

I/O RAM DESCRIPTION – Alphabetical Order

Bits with a W (write) direction are written by the MPU into configuration RAM. Typically, they are initially stored in flash memory and copied to the configuration RAM by the MPU. Some of the more frequently programmed bits are mapped to the MPU SFR memory space. The remaining bits are mapped to 2xxx. Bits with R (read) direction can be read by the MPU. On power up, all bits are cleared to zero unless otherwise stated.

NAME	LOCATION	DIR	DESCRIPTION																											
<i>ADC_DIS</i>	2005[3]	R/W	Disables ADC and removes bias current																											
<i>CE_EN</i>	2000[4]	R/W	CE enable.																											
<i>CHOP_EN[1:0]</i>	2002[5:4]	R/W	Chop enable for the reference band gap circuit. 00-enabled 01-disabled 10-disabled 11-enabled																											
<i>RESERVED</i>	2004[5]	R/W	Must be 0.																											
<i>CKOUT_DIS</i>	2004[4]	R/W	CKOUT Disable. When zero, CKTEST is an active output.																											
<i>RESERVED</i>	2003[4:3]	R/W	Must be 00																											
<i>DIO_R4[2:0]</i> <i>DIO_R5[2:0]</i> <i>DIO_R6[2:0]</i> <i>DIO_R7[2:0]</i> <i>DIO_R8[2:0]</i> <i>DIO_R9[2:0]</i> <i>DIO_R10[2:0]</i> <i>DIO_R11[2:0]</i>	200B[2:0] 200B[6:4] 200C[2:0] 200C[6:4] 200D[2:0] 200D[6:4] 200E[2:0] 200E[6:4]	R/W	Connects dedicated I/O pins 4 to 11 to internal resources. If more than one input is connected to the same resource, the 'MULTIPLE' column below specifies how they are combined. <table border="1" data-bbox="743 1094 1495 1518"> <thead> <tr> <th>DIO_GP</th> <th>Resource</th> <th>MULTIPLE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NONE</td> <td>--</td> </tr> <tr> <td>1</td> <td>Reserved</td> <td>OR</td> </tr> <tr> <td>2</td> <td>T0 (counter0 clock)</td> <td>OR</td> </tr> <tr> <td>3</td> <td>T1 (counter1 clock)</td> <td>OR</td> </tr> <tr> <td>4</td> <td>High priority IO interrupt (int0 rising)</td> <td>OR</td> </tr> <tr> <td>5</td> <td>Low priority IO interrupt (int1 rising)</td> <td>OR</td> </tr> <tr> <td>6</td> <td>High priority IO interrupt (int0 falling)</td> <td>OR</td> </tr> <tr> <td>7</td> <td>Low priority IO interrupt (int1 falling)</td> <td>OR</td> </tr> </tbody> </table>	DIO_GP	Resource	MULTIPLE	0	NONE	--	1	Reserved	OR	2	T0 (counter0 clock)	OR	3	T1 (counter1 clock)	OR	4	High priority IO interrupt (int0 rising)	OR	5	Low priority IO interrupt (int1 rising)	OR	6	High priority IO interrupt (int0 falling)	OR	7	Low priority IO interrupt (int1 falling)	OR
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3	T1 (counter1 clock)	OR																												
4	High priority IO interrupt (int0 rising)	OR																												
5	Low priority IO interrupt (int1 rising)	OR																												
6	High priority IO interrupt (int0 falling)	OR																												
7	Low priority IO interrupt (int1 falling)	OR																												
<i>RESERVED</i>	2009..200A	R/W	Must be 0000.																											
<i>RESERVED</i>	SFRA2[3:0]	R/W	Must be 1111.																											

<i>DIO_DIR0</i> [7:4]	SFRA2[7:4]	R/W	<p>Programs the direction of DIO pins 7 through 4. 1 indicates output. Ignored if the pin is not configured as I/O. See <i>DIO_PV</i> and <i>DIO_PW</i> for special option for DIO_6 and DIO_7 outputs. See <i>DIO_EEX</i> for special option for DIO_4 and DIO_5.</p> <p>Note: Bit 0, Bit 1, Bit 2 and Bit 3 must be set to 1.</p>
<i>DIO_DIR1</i> [7:6] <i>DIO_DIR1</i> [3:0]	SFR91	R/W	<p>Programs the direction of DIO pins 15, 14 and 11 through 8. 1 indicates output. Ignored if the pin is not configured as I/O.</p> <p>Note: Bit 4 and Bit 5 must be set to 1.</p>
<i>DIO_DIR2</i> [1:0]	SFRA1[5:0]	R/W	<p>Programs the direction of DIO pins 17 and 16. 1 indicates output. Ignored if the pin is not configured as I/O.</p> <p>Note: Bit 2, Bit 3, Bit 4 and Bit 5 must be set to 1.</p>
<i>DIO_0</i> [7:4] <i>DIO_1</i> [7:6], <i>DIO_1</i> [3:0] <i>DIO_2</i> [1:0]	SFR80 SFR90 SFRA0[1:0]	R/W	<p>The value on the DIO pins. Pins configured as LCD will read zero. When written, changes data on pins configured as outputs. Pins configured as LCD or input will ignore writes.</p>
<i>DIO_EEX</i>	2008[4]	R/W	<p>When set, converts DIO_4 and DIO_5 to interface with external EEPROM. DIO_4 becomes SCL and DIO_5 becomes bi-directional SDA. <i>LCD_NUM</i> must be less than 17.</p>
<i>DIO_PV</i>	2008[2]	R/W	<p>Causes VARPULSE to be output on DIO_7, if DIO_7 is configured as output. <i>LCD_NUM</i> must be less than 15.</p>
<i>DIO_PW</i>	2008[3]	R/W	<p>Causes WPULSE to be output on DIO_6, if DIO_6 is configured as output. <i>LCD_NUM</i> must be less than 16.</p>
<i>EEDATA</i> [7:0]	SFR9E	R/W	Serial EEPROM interface data
<i>EECTRL</i> [7:0]	SFR9F	R/W	Serial EEPROM interface control
<i>ECK_DIS</i>	2005[5]	R/W	Emulator clock disable. When one, the emulator clock is disabled.
<i>EQU</i> [2:0]	2000[7:5]	R/W	Specifies the power equation.
<i>EX_XFR</i> <i>EX_RTC</i>	2002[0] 2002[1]	R/W	Interrupt enable bits. These bits enable the XFER_BUSY and the RTC_1SEC interrupts. Note that if either interrupt is to be enabled, EX6 in the 80515 must also be set.
<i>FIR_LEN</i>	2005[4]	R/W	<p>The length of the ADC decimation FIR filter.</p> <p>1 - 22 ADC bits/3 CK32 cycles 0 - 21 ADC bits/2 CK32 cycles</p>

<i>FLASH66Z</i>	2005[1]	R/W	Should be set to 1 to minimize power supply current.
<i>FLSH_ERASE</i>	SFR94	W	<u>Flash Erase Initiate</u> <i>FLSH_ERASE</i> is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for <i>FLSH_ERASE</i> in order to initiate the appropriate Erase cycle. (default = 0x00). 0x55 – Initiate Flash Page Erase cycle. Must be preceded by a write to <i>FLSH_PGADR</i> @ sfr 0xB7. 0xAA – Initiate Flash Mass Erase cycle. Must be preceded by a write to <i>FLSH_MEEN</i> @ sfr 0xB2 and the debug (CC) port must be enabled. Any other pattern written to <i>FLSH_ERASE</i> will have no effect.
<i>FLSH_MEEN</i>	SFRB2[1]	W	<u>Mass Erase Enable</u> 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. <i>Must be re-written for each new Mass Erase cycle.</i>
<i>FLSH_PGADR</i>	SFRB7[7:1]	W	<u>Flash Page Erase Address</u> <i>FLSH_PGADR</i> [6:0] – Flash Page Address (page 0 thru 127) that will be erased during the Page Erase cycle. (default = 0x00). <i>Must be re-written for each new Page Erase cycle.</i>
<i>FLSH_PWE</i>	SFRB2[0]	R/W	<u>Program Write Enable</u> 0 – MOVX commands refer to External RAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to External Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
<i>IE_XFER</i> <i>IE_RTC</i>	SFRE8[0] SFRE8[1]	R/W	Interrupt flags. These flags monitor the XFER_BUSY interrupt and the RTC_1SEC interrupt. The flags are set by hardware and must be cleared by the interrupt handler.
<i>INTBITS</i>	SFRF8[6:0]	R	Interrupt inputs. The MPU may read these bits to see the input to external interrupts INT0, INT1, up to INT6. These bits do not have any memory and are primarily intended for debug use.

<i>LCD_BSTEN</i>	2020[7]	R/W	Enables the LCD voltage boost circuit.																																										
<i>LCD_CLK</i> [1:0]	2021[1:0]	R/W	Sets the LCD clock frequency. Note: $fw = CKADC/128$ 00: $w/2^9$, 01: $fw/2^8$, 10: $fw/2^7$, 11: $fw/2^6$																																										
<i>LCD_EN</i>	2021[5]	R/W	Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs.																																										
<i>LCD_FS</i> [4:0]	2022[4:0]	R/W	The LCD full scale voltage, VLC2. 00 is $(0.7 * VLCD)$ and 1F is VLCD																																										
<i>LCD_MODE</i> [2:0]	2021[4:2]	R/W	The LCD bias mode: 000-4 states, 1/3 bias 001-3 states, 1/3 bias 010-2 states, 1/2 bias 011-3 states, 1/2 bias 100-static display																																										
<i>LCD_NUM</i> [4:0]	2020[4:0]	R/W	Controls the number of dual-purpose LCD/DIO pins to be configured as LCD. <i>LCD_NUM</i> will be between 0 and 18. The first dual-purpose pin to be allocated as LCD is SEG37/DIO17. The table below lists which SEG and DIO functions are selected for each <i>LCD_NUM</i> value.																																										
			<table border="1"> <thead> <tr> <th><i>LCD_NUM</i></th> <th>SEG</th> <th>DIO</th> </tr> </thead> <tbody> <tr> <td>1-4</td> <td>None</td> <td>DIO4-11, DIO14-17</td> </tr> <tr> <td>5</td> <td>SEG37</td> <td>DIO4-11, DIO14-16</td> </tr> <tr> <td>6</td> <td>SEG36-37</td> <td>DIO4-11, DIO14-15</td> </tr> <tr> <td>7</td> <td>SEG35-37</td> <td>DIO4-11, DIO14</td> </tr> <tr> <td>8-10</td> <td>SEG34-37</td> <td>DIO4-11</td> </tr> <tr> <td>11</td> <td>SEG34-37, SEG31</td> <td>DIO4-10</td> </tr> <tr> <td>12</td> <td>SEG34-37, SEG30-31</td> <td>DIO4-9</td> </tr> <tr> <td>13</td> <td>SEG34-37, SEG29-31</td> <td>DIO4-8</td> </tr> <tr> <td>14</td> <td>SEG34-37, SEG28-31</td> <td>DIO4-7</td> </tr> <tr> <td>15</td> <td>SEG34-37, SEG27-31</td> <td>DIO4-6</td> </tr> <tr> <td>16</td> <td>SEG34-37, SEG26-31</td> <td>DIO4-5</td> </tr> <tr> <td>17</td> <td>SEG34-37, SEG25-31</td> <td>DIO4</td> </tr> <tr> <td>18</td> <td>SEG34-37, SEG24-31</td> <td>None</td> </tr> </tbody> </table>	<i>LCD_NUM</i>	SEG	DIO	1-4	None	DIO4-11, DIO14-17	5	SEG37	DIO4-11, DIO14-16	6	SEG36-37	DIO4-11, DIO14-15	7	SEG35-37	DIO4-11, DIO14	8-10	SEG34-37	DIO4-11	11	SEG34-37, SEG31	DIO4-10	12	SEG34-37, SEG30-31	DIO4-9	13	SEG34-37, SEG29-31	DIO4-8	14	SEG34-37, SEG28-31	DIO4-7	15	SEG34-37, SEG27-31	DIO4-6	16	SEG34-37, SEG26-31	DIO4-5	17	SEG34-37, SEG25-31	DIO4	18	SEG34-37, SEG24-31	None
<i>LCD_NUM</i>	SEG	DIO																																											
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<i>LCD_SEG0</i> [3:0]- <i>LCD_SEG19</i> [3:0], <i>LCD_SEG24</i> [3:0]- <i>LCD_SEG31</i> [3:0], <i>LCD_SEG34</i> [3:0]- <i>LCD_SEG37</i> [3:0],	2030[3:0]- 2043[3:0], 2048[3:0]- 204f[3:0], 2052[3:0]- 2055[3:0]	R/W	LCD Segment Data. Each word contains information for from 1 to 4 time divisions of each segment. In each word, bit 0 corresponds to COM0, on up to bit 3 for COM3.
<i>MPU_DIV</i> [2:0]	2004[2:0]	R/W	The MPU clock divider (from CKCE). These bits may be programmed by MPU without risk of losing control. $000\text{-CKCE}, 001\text{-CKCE}/2, \dots, 111\text{-CKCE}/2^7$
<i>MUX_ALT</i>	2005[2]	R/W	The MPU asserts this bit when it wishes the MUX to perform ADC conversions on an alternate set of inputs.
<i>MUX_DIV</i> [1:0]	2002[7:6]	R/W	The number of states in the input mux. 00: 6 states 01: 4 states 10: 3 states 11: 2 states
<i>MUX_E</i>	2005[0]	R/W	<i>MUX_SYNC</i> enable. When high, converts SEG7 into a <i>MUX_SYNC</i> output.
<i>OPT_TXDIS</i>	2008[5]	R/W	Tristates the <i>OPT_TX</i> output.
<i>PREBOOT</i>	SFRB2[7]	R	Indicates that preboot sequence is active.
<i>PRE_SAMPS</i> [1:0]	2001[7:6]	R/W	Together w/ <i>SUM_CYCLES</i> , this value determines the number of samples in one sum cycle between XFER interrupts. Number of cycles = <i>PRE_SAMPS</i> * <i>SUM_CYCLES</i> . 00-42, 01-50, 10-84, 11-100
<i>RTC_SEC</i> [5:0] <i>RTC_MINI</i> [5:0] <i>RTC_HR</i> [4:0] <i>RTC_DAY</i> [2:0] <i>RTC_DATE</i> [4:0] <i>RTC_MO</i> [3:0] <i>RTC_YR</i> [7:0]	2015 2016 2017 2018 2019 201A 201B	R/W	The RTC interface. These are the 'year', 'month', 'day', 'hour', 'minute' and 'second' parameters for the RTC. The RTC is set by writing to these registers. Year 00 is defined as a leap year. SEC 00 to 59 MIN 00 to 59 HR 00 to 23 (00=Midnight) DAY 01 to 07 (01=Sunday) DATE 01 to 31 MO 01 to 12 YR 00 to 255

<i>RTC_DEC_SEC</i> <i>RTC_INC_SEC</i>	201C[1] 201C[0]	W	RTC time correction bits. Only one bit may be pulsed at a time. When pulsed, causes the RTC time value to be incremented (or decremented) by an additional second the next time the <i>RTC_SEC</i> register is clocked. The pulse width may be any value. If an additional correction is desired, the MPU must wait 2 seconds before pulsing one of the bits again.
<i>RTM_EN</i>	2002[3]	R/W	Real Time Monitor enable. When '0', the RTM output is low. This bit enables the two wire version of RTM
<i>RTM0[7:0]</i> <i>RTM1[7:0]</i> <i>RTM2[7:0]</i> <i>RTM3[7:0]</i>	2060 2061 2062 2063	R/W	Four RTM probes. Before each CE code pass, the values of these registers are serially output on the RTM pin. The <i>RTM</i> registers are ignored when <i>RTM_EN</i> =0.
<i>SECURE</i>	SFRB2[6]	R/W	Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
<i>SSI_EN</i>	2070[7]	R/W	Enables the Synchronous Serial Interface (SSI) on SEG3, SEG4, and SEG5 pins. If <i>SSI_RDYEN</i> is set, SEG6 is enabled also. The pins take on the new functions SCLK, SSDATA, SFR, and SRDY, respectively. When <i>SSI_EN</i> is high and <i>LCD_EN</i> is low, these pins are converted to the SSI function, regardless of <i>LCDEN</i> and <i>LCD_NUM</i> . For proper LCD operation, <i>SSI_EN</i> must not be high when <i>LCD_EN</i> is high.
<i>SSI_10M</i>	2070[6]	R/W	SSI clock speed: 0-5MHz 1-10MHz
<i>SSI_CKGATE</i>	2070[5]	R/W	SSI gated clock enable. When low, the SCLK is continuous. When high, the clock is held low when data is not being transferred.
<i>SSI_FSIZE[1:0]</i>	2070[4:3]	R/W	SSI frame pulse format: 0: once at beginning of SSI sequence (whole block of data), 1: every 8 bits, 2: every 16 bits, 3: every 32 bits.
<i>SSI_FPOL</i>	2070[2]	R/W	SFR pulse polarity: 0-positive 1-negative
<i>SSI_RDYEN</i>	2070[1]	R/W	SRDY enable. If <i>SSI_RDYEN</i> and <i>SSI_EN</i> are high, the SEG6 pin is configured as SRDY. Otherwise, it is an LCD driver.
<i>SSI_RDYPOL</i>	2070[0]	R/W	SRDY polarity: 0-positive 1-negative
<i>SSI_BEG[7:0]</i> <i>SSI_END[7:0]</i>	2071[7:0] 2072[7:0]	R/W	The beginning and ending address of the transfer region of the CE data memory. If Synchronous Serial Interface is enabled, a block of words starting with <i>SSI_BEG</i> and ending with <i>SSI_END</i> will be sent. <i>SSI_END</i> must be larger than <i>SSI_BEG</i> . The maximum number of output words is limited by the number of SSI clocks in a CE code pass—see <i>FIR_LEN</i> , <i>MUX_DIV</i> , and <i>SSI_10M</i> .

<i>SUM_CYCLES</i> [5:0]	2001[5:0]	R/W	Together w/ <i>PRE_SAMPS</i> , this value determines the number of samples in one sum cycle between XFER interrupts. Number of cycles = <i>PRE_SAMPS</i> * <i>SUM_CYCLES</i> .
<i>TMUX</i> [3:0]	2000[3:0]	R/W	Selects one of 16 inputs for TMUXOUT. 0 – DGND (analog) 1 – IBIAS (analog) 2 – PLL_2.5v (analog) 3 – VBIAS (analog) 4 – RTM (Real time output from CE) 5 – WDTR_EN (Comparator 1 Output AND V1LT3) 6 – Reserved 7 – Reserved 8 – RXD (from Optical interface) 9 – MUX_SYNC (from MUX_CTRL) A – CK_10M B – CK_MPU C – Reserved D – RTCLK E – CE_BUSY F – XFER_BUSY
<i>RESERVED</i>	2005[7]	R/W	Must be Zero.
<i>TRIMSEL</i>	20FD	W	Selects the temperature trim fuse to be read with the <i>TRIM</i> register (<i>TRIMM</i> [2:0]: 4, <i>TRIMBGA</i> : 5, <i>TRIMBGB</i> : 6)
<i>TRIM</i>	20FF	R	Contains <i>TRIMBGA</i> , <i>TRIMBGB</i> , or <i>TRIMM</i> [2:0] depending on the value written to <i>TRIMSEL</i> . If <i>TRIMBGB</i> = 0 then the IC is a 6511 else the IC is a 6511H.
<i>VERSION</i> [7:0]	2006	R	The silicon revision number. This data sheet does not apply to revisions < 0000 0100.
<i>VREF_CAL</i>	2004[7]	R/W	Makes voltage reference available to VREF pin. This feature is disabled when <i>VREF_DIS</i> =1.
<i>VREF_DIS</i>	2004[3]	R/W	Disables the internal voltage reference.

<i>WD_RST</i>	SFRE8[7]	W	Reset the WD timer. The WD is reset when a 1 is written to this bit.
<i>WD_OVF</i>	2002[2]	R/W	The WD overflow status bit. This bit is set when the WD timer overflows. It is powered by the NV supply and at bootup will indicate if the part is recovering from a WD overflow or a power fault. This bit should be cleared by the MPU on bootup. It is also automatically cleared when RESETZ is low.

I/O RAM MAP – In Numerical Order

'Not Used' bits are blacked out, contain no memory and are read by the MPU as zero. *RESERVED* bits are in use and should not be changed. This table lists only the SFR registers that are not generic 8051 SFR registers.

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Configuration:										
CE0	2000	EQU[2:0]			CE_EN	TMUX[3:0]				
CE1	2001	PRE_SAMPS[1:0]		SUM_CYCLES[5:0]						
CE2	2002	MUX_DIV[1:0]		CHOP_EN[1:0]		RTM_EN	WD_OVF	EX_RTC	EX_XFR	
COMP0	2003			RESERVED		RESERVED				
CONFIG0	2004	VREF_CAL		RESERVED	CKOUT_DIS	VREF_DIS	MPU_DIV			
CONFIG1	2005	RESERVED		ECK_DIS	FIR_LEN	ADC_DIS	MUX_ALT	FLSH66Z	MUX_E	
VERSION	2006	VERSION[7:0]								
Digital I/O:										
DIO0	2008			OPT_TXDIS	DIO_EEX	DIO_PW	DIO_PV	RESERVED		
DIO1	2009	RESERVED								
DIO2	200A	RESERVED								
DIO3	200B	DIO_R5[2:0]				DIO_R4[2:0]				
DIO4	200C	DIO_R7[2:0]				DIO_R6[2:0]				
DIO5	200D	DIO_R9[2:0]				DIO_R8[2:0]				
DIO6	200E	DIO_R11[2:0]				DIO_R10[2:0]				
DIO7	SFR80	DIO_0[7:4]				RESERVED				
DIO8	SFR92	DIO_DIR0[7:4]				1111				
DIO9	SFR90	DIO_1[7:6]		RESERVED			DIO_1[3:0]			
DIO10	SFR91	DIO_DIR1[7:6]		11			DIO_DIR1[3:0]			
DIO11	SFRA0	RESERVED				DIO_2[1:0]				
DIO12	SFRA1	1111				DIO_DIR2[1:0]				
Interrupts and WD Timer:										
INTBITS	SFRF8		INT6	INT5	INT4	INT3	INT2	INT1	INT0	
WDI	SFRE8	WD_RST						IE_RTC	IE_XFER	
Flash:										
ERASE	SFR94	FLSH_ERASE[7:0]								
FLSHCTL	SFRB2	PREBOOT	SECURE					FLSH_MEEN	FLSH_PWE	
PGADR	SFRB7	FLSH_PGADR[6:0]								
Real Time Clock:										
RTC0	2015					RTC_SEC[5:0]				
RTC1	2016					RTC_MIN[5:0]				
RTC2	2017					RTC_HR[4:0]				
RTC3	2018					RTC_DAY[2:0]				
RTC4	2019					RTC_DATE[4:0]				
RTC5	201A					RTC_MO[3:0]				
RTC6	201B	RTC_YR[7:0]								
RTC7	201C							RTC_DEC_SEC	RTC_INC_SEC	
LCD Display Interface:										
LCDX	2020	LCD_BSTEM			LCD_NUM[4:0]					
LCDY	2021			LCD_EN	LCD_MODE[2:0]			LCD_CLK[1:0]		
LCDZ	2022				LCD_FS[4:0] RESERVED:SEG20-23,32-33,38-41					
LCD0	2030					LCD_SEG0[3:0]				
LCD1	2031					LCD_SEG1[3:0]				
...				
LCD19	2043					LCD_SEG19[3:0]				
LCD20	2044	RESERVED								
LCD21	2045	RESERVED								
LCD22	2046	RESERVED								
LCD23	2047	RESERVED								

LCD24	2048									<i>LCD_SEG24[3:0]</i>
LCD25	2049									<i>LCD_SEG25[3:0]</i>
LCD26	204A									<i>LCD_SEG26[3:0]</i>
LCD27	204B									<i>LCD_SEG27[3:0]</i>
LCD28	204C									<i>LCD_SEG28[3:0]</i>
LCD29	204D									<i>LCD_SEG29[3:0]</i>
LCD30	204E									<i>LCD_SEG30[3:0]</i>
LCD31	204F									<i>LCD_SEG31[3:0]</i>
LCD32	2050									<i>RESERVED</i>
LCD33	2051									<i>RESERVED</i>
LCD34	2052									<i>LCD_SEG34[3:0]</i>
LCD35	2053									<i>LCD_SEG35[3:0]</i>
LCD36	2054									<i>LCD_SEG36[3:0]</i>
LCD37	2055									<i>LCD_SEG37[3:0]</i>
LCD38	2056									<i>RESERVED</i>
LCD39	2057									<i>RESERVED</i>
LCD40	2058									<i>RESERVED</i>
LCD41	2059									<i>RESERVED</i>
RTM Probes:										
RTM0	2060									<i>RTM0[7:0]</i>
RTM1	2061									<i>RTM1[7:0]</i>
RTM2	2062									<i>RTM2[7:0]</i>
RTM3	2063									<i>RTM3[7:0]</i>
Synchronous Serial Interface:										
SSI	2070	<i>SSI_EN</i>	<i>SSI_10M</i>	<i>SSI_CKGATE</i>	<i>SSI_FSIZE[1:0]</i>	<i>SSI_FPOL</i>	<i>SSI_RDYEN</i>	<i>SSI_RDYPOL</i>		
SSI_BEG	2071									<i>SSI_BEG[7:0]</i>
SSI_END	2072									<i>SSI_END[7:0]</i>
Serial EEPROM:										
EEDATA	SFR9E									<i>EEDATA[7:0]</i>
EECTRL	SFR9F									<i>EECTRL[7:0]</i>
Fuse Selection Registers:										
TRIMSEL	20FD									<i>TRIMSEL[7:0]</i>
TRIM	20FF									<i>TRIM[7:0]</i>

CE Interface Description
FORMATS

All CE words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement. 'Calibration' parameters are defined in flash memory (or external EEPROM) and must be copied to CE memory by the MPU before enabling the CE. 'Internal' variables are used in internal CE calculations. 'Input' variables allow the MPU to control the behavior of the CE code. 'Output' variables are outputs of the CE calculations. The corresponding MPU address for the most significant byte is given by 1000 (hex) + 4 x CE_address and 1003 (hex) + 4 x CE_address for the least significant byte.

Note: The information given in the following tables apply to CE code Version CE11B04.

CE Internal Data:		
<i>First CE Address</i>	5D	First CE memory location
...
<i>Last CE Address</i>	FF	Last CE memory location

CONSTANTS

Constants used in the CE Data Memory tables are:

- $F_s = 32768\text{Hz}/13 = 2520.62\text{Hz}$.
- F_0 is the fundamental frequency.
- $IMAX$ is the external rms current corresponding to 250mV pk at the inputs IA and IB.
- $VMAX$ is the external rms voltage corresponding to 250mV pk at the VA input.
- $NACC$, the accumulation count for energy measurements is $PRE_SAMPS * SUM_CYCLES$.
- Accumulation count time for energy measurements is $PRE_SAMPS * SUM_CYCLES / F_s$.

The system constants $IMAX$ and $VMAX$ are used by the MPU to convert internal quantities (as used by the CE) to external, i.e. metering quantities. Their values are determined by the scaling of the voltage and current sensors used in an actual meter. $IMAX$ and $VMAX$ are specified in this datasheet for reference only. The LSB values used in this document relate digital quantities at the CE or MPU interface to external meter input quantities. For example, if a SAG threshold of 80V peak is desired at the meter input, the digital value that should be programmed into SAG_THR would be $80V / SAG_THR_{LSB}$, where SAG_THR_{LSB} is the LSB value in the description of SAG_THR .

The parameters EQU , CE_EN , PRE_SAMPS , and SUM_CYCLES essential to the function of the CE are stored in I/O RAM (see I/O RAM section).

ENVIRONMENT

Before starting the CE using the CE_EN bit, the MPU has to establish the proper environment for the CE by implementing the following steps:

- Loading the image for the CE code into CE PRAM.
- Loading the CE data into CE DRAM.
- Establishing the equation to be applied in EQU .
- Establishing the accumulation period and number of samples in PRE_SAMPS and SUM_CYCLES .
- Establishing the number of cycles per ADC mux frame.

There must be thirteen 32768Hz cycles per ADC mux frame (see System Timing Diagram, Figure 7). This means that the product of the number of cycles per frame and the number of conversions per frame must be 12 (allowing for one settling cycle). The default configuration is *FIR_LEN* = 1 (three cycles per conversion) and *MUX_DIV* = 1 (4 conversions per mux frame).

During operation, the MPU is in charge of controlling the multiplexer cycles, for example by inserting an alternative multiplexer sequence at regular intervals using *MUX_ALT*. This enables temperature measurement. The polarity of CHOP must be altered for each sample. It must also alternate for each Alt Mux reading.

The MPU must program *CHOP_EN* alternately between 01 and 10 on every *CE_BUSY* interrupt except for the first *CE_BUSY* after an *XFER_BUSY* interrupt. Note that when *XFER_BUSY* occurs, it will always be at the same time as a *CE_BUSY* interrupt.

CE CALCULATIONS

The CE performs the precision computations necessary to accurately measure power. These computations include offset cancellation, products, product smoothing, product summation, frequency detection, VAR calculation, sag detection, peak detection, and voltage phase measurement. All data computed by the CE is dependent on the selected meter equation as given by *EQU* (in I/O RAM).

<i>EQU</i>	Watt & VAR Formula (WSUM/VARSUM)	Element Input Mapping			
		<i>W0SUM</i> / <i>VAR0SUM</i>	<i>W1SUM</i> / <i>VAR1SUM</i>	<i>I0SQSUM</i>	<i>I1SQSUM</i>
0	VA IA (1 element, 2W 1φ)	VA*IA	VA*IB	IA	IB
1	VA*(IA-IB)/2 (1 element, 3W 1φ)	VA*(IA-IB)/2	VA*IB	IA-IB	IB

CE STATUS WORD

Since the *CE_BUSY* interrupt occurs at 2520.6Hz, it is desirable to minimize the computation required in the interrupt handler of the MPU. The CE status word can be read by the MPU at every *CE_BUSY* interrupt.

CE Address	Name	Description
51	<i>CESTATUS</i>	See description of CE status word below

The CE Status Word has been created for generating early warnings to the MPU. It contains sag warnings for VA as well as F0, the derived clock operating at the fundamental input frequency. *CESTATUS* provides information about the status of voltage and input AC signal frequency which are useful generating early power fail warning to initiate necessary data storage. *CESTATUS* represents the status flags for the preceding CE code pass (CE busy interrupt). Sag alarms are not remembered from one code pass to the next. The CE Status word is refreshed at every *CE_BUSY* interrupt.

The significance of the bits in *CESTATUS* is shown in the table below:

CESTATUS [bit]	Name	Description
31-29	Not Used	These unused bits will always be zero.
28	<i>F0</i>	<i>F0</i> is a square wave at the exact fundamental input frequency.
27	<i>RESERVED</i>	
26	<i>RESERVED</i>	
25	<i>SAG_A</i>	Normally zero. Becomes one when VA remains below <i>SAG_THR</i> for <i>SAG_CNT</i> samples. Will not return to zero until VA rises above <i>SAG_THR</i> .
24-0	Not Used	These unused bits will always be zero.

For generating proper status information the CE has to be initialized by the MPU using *SAG_THR* (default of 80V RMS at the meter input, if *VMAX*=600V) and *SAG_CNT* (default 80 samples). To activate the *SAG* status bit, the peak-to-peak signal has to be below *SAG_THR* value for 32 milliseconds.

CE Address	Name	Default	Description
31	<i>SAG_THR</i>	+56,722,300 (0x361837C)	Meter voltage inputs must be above this threshold to prevent sag alarms. LSB = $V_{MAX} * 3.3243 * 10^{-9}$ Vpk. For example, if a sag threshold of 80V RMS is desired, $SAG_THR = \frac{80\sqrt{2}}{V_{MAX} \cdot 3.3243 \cdot 10^{-9}}$
32	<i>SAG_CNT</i>	80	Number of consecutive voltage samples below <i>SAG_THR</i> before a sag alarm is declared.

CE TRANSFER VARIABLES

When the MPU receives the *XFER_BUSY* interrupt, it knows that fresh data is available in the transfer variables. The transfer variables can be categorized as:

1. Fundamental power measurement variables
2. Instantaneous (RMS) values
3. Other measurement parameters
4. Temperature measurement variables
5. Pulse generation variables
6. Current shunt variables
7. Calibration parameters

Fundamental Power Measurement Variables

The table below describes each transfer variable for fundamental power measurement. All variables are signed 32 bit integers. Accumulated variables such as WSUM are internally scaled so they have at least 2x margin before overflow when the integration time is 1 second. Additionally, the hardware will not permit output values to 'fold back' upon overflow.

CE Address	Name	Description
42	RESERVED	
43	W0SUM_X	The sum of Watt samples from each wattmeter element (I_{n_8} is the gain configured by IA_SHUNT or IB_SHUNT). LSB = $6.6952 \times 10^{-13} V_{MAX} I_{MAX} / I_{n_8}$ Wh.
44	W1SUM_X	
45	RESERVED	
46	RESERVED	
47	VAR0SUM_X	The sum of VAR samples from each wattmeter element (I_{n_8} is the gain configured by IA_SHUNT or IB_SHUNT). LSB = $6.6952 \times 10^{-13} V_{MAX} I_{MAX} / I_{n_8}$ Wh.
48	VAR1SUM_X	
49	RESERVED	

$WxSUM_X$ is the Wh value accumulated for element 'X' in the last accumulation interval and can be computed based on the specified LSB value.

For example with $V_{MAX} = 600V$ and $I_{MAX} = 208A$, LSB (for $WxSUM_X$) is $0.08356 \mu Wh$.

Instantaneous Power Measurement Variables

The Frequency measurement is computed using the Frequency locked loop for the selected phase.

$IxSQSUM_X$ and $VxSQSUM$ are the squared current and voltage samples acquired during the last accumulation interval.

$INSQSUM_X$ can be used for computing the neutral current.

CE Address	Name	Description
33	RESERVED	
41	FREQ_X	Fundamental frequency. $LSB \equiv \frac{F_S}{2^{32}} \approx 0.587 \cdot 10^{-6} \text{ Hz}$
4A	I0SQSUM_X	The sum of squared current samples from each element. $LSB = 6.6952 \cdot 10^{-13} I_{MAX}^2 / \ln_8^2 A^2 h$
4B	I1SQSUM_X	
4C	RESERVED	
4D	RESERVED	
4E	V0SQSUM_X	The sum of squared voltage samples from each element. $LSB = 6.6952 \cdot 10^{-13} V_{MAX}^2 V^2 h$
4F	RESERVED	
50	RESERVED	

The RMS values can be computed by the MPU from the squared current and voltage samples as per the formula

$$I_{xRMS} = \text{SQRT}(I_{xSQSUM} * LSB * 3600 * F_S / N_{ACC})$$

$$V_{xRMS} = \text{SQRT}(V_{xSQSUM} * LSB * 3600 * F_S / N_{ACC})$$

Other Measurement Parameters

MAINEDGE_X is useful for implementing a real-time clock based on the input AC signal. *MAINEDGE_X* is the number of half-cycles accounted for in the last accumulated interval for the AC signal.

CE Address	Name	Description
52	RESERVED	
53	RESERVED	
55	MAINEDGE_X	The number of edge crossings of the selected voltage in the previous accumulation interval. Edge crossings are either direction and are debounced.

Temperature Measurement

Input variables: *TEMP_NOM* is the reference value for temperature measurement. That is when this value is set with *TEMP_RAW_X* at known temperature. The 71M6511 measures temperature with reference to this value.

DEGSCALE is the slope or rate of temperature increase or decrease from the *TEMP_NOM* for *TEMP_X* measurement.

PPMC and *PPMC2* are temperature compensation coefficients. Their values should reflect the band gap voltage reference characteristics of the chip. *PPMC* and *PPMC2* follow the square law characteristics to compensate for nonlinear temperature behaviors.

CE Address	Name	Default	Description
11	<i>TEMP_NOM</i>	0	During calibration, the value of <i>TEMP_RAW_X</i> should be placed in <i>TEMP_NOM</i> .
30	<i>DEGSCALE</i>	9585	Scale factor for <i>TEMP_X</i> . $TEMP_X = -DEGSCALE * 2^{-22} * (TEMP_RAW_X - TEMP_NOM)$.
38	<i>EXT_TEMP</i>	0	Should be 15 or 0. When 15, causes the CE to ignore internal temperature compensation and permits the MPU to control <i>GAIN_ADJ</i> . When internal temperature compensation is selected <i>GAIN_ADJ</i> will be: $GAIN_ADJ = 16385 + \frac{TEMP_X \cdot PPMC}{2^{14}} + \frac{TEMP_X^2 \cdot PPMC2}{2^{23}}$ Default is 0 (internal compensation).
39	<i>PPMC</i>	0	$PPMC * 26.84$. Linear temperature compensation. A positive value will cause the meter to run faster when hot. This is applied to both V and I and will therefore have a double effect on products.
3A	<i>PPMC2</i>	0	$PPMC^2 * 1374$. Square-law compensation. A positive value will cause the meter to run faster when hot. This is applied to both V and I and will therefore have a double effect on products.

Output variables: *TEMP_X* is the temperature measurement from reference temperature of *TEMP_NOM*. *TEMP_X* is computed using *TEMP_RAW_X* and *DEGSCALE*. This quantity is positive when the temperature is above the reference and is negative for cold temperatures.

TEMP_RAW_X is the raw processed value from ADC output and is the fundamental quantity for temperature measurement. *TEMP_RAW_X* is less than *TEMP_NOM* at higher temperatures. *TEMP_RAW_X* is more than *TEMP_NOM* for cooler temperatures than reference temperature.

GAIN_ADJ is a scaling factor power measurements based on the temperatures. In general, for higher temperatures is lower than 16384 and is higher than 16384 for colder temperatures. *GAIN_ADJ* is mainly dependent on the *PPMC*, *PPMC2* and *TEMP_X* register values. This parameter is automatically computed by the CE and is used by CE the for temperature compensation.

CE Address	Name	Description
40	<i>TEMP_X</i>	Deviation from Calibration temperature. LSB = 0.1 °C.
54	<i>TEMP_RAW_X</i>	Filtered, unscaled reading from temperature sensor. This value should be written to <i>TEMP_NOM</i> during meter calibration.
2E	<i>GAIN_ADJ</i>	Scales all voltage and current inputs. 16384 provides unity gain. Default is 16384

Pulse Generation

Input variables: *PULSE_SLOW* and *PULSE_FAST* parameters control the speed of the pulse rate individually and also together. Default values of 1 and 1 result will maintain the original pulse rate given by the kh equation.

CE Address	Name	Default	Description															
28	<i>PULSE_SLOW</i>	1	When <i>PULSE_SLOW</i> > 0, the pulse generator input is reduced 64x. When <i>PULSE_FAST</i> > 0, the pulse generator input is increased 16x. These two parameters control the pulse gain factor X (see table below). Allowed values are either 1 or -1. Default is 1. <table border="1" data-bbox="743 1115 1484 1335"> <thead> <tr> <th>X</th> <th><i>PULSE_SLOW</i></th> <th><i>PULSE_FAST</i></th> </tr> </thead> <tbody> <tr> <td>$1.5 * 2^2 = 6$</td> <td>-1</td> <td>-1</td> </tr> <tr> <td>$1.5 * 2^6 = 96$</td> <td>-1</td> <td>1</td> </tr> <tr> <td>$1.5 * 2^{-4} = 0.09375$</td> <td>1</td> <td>-1</td> </tr> <tr> <td>1.5</td> <td>1 (default)</td> <td>1 (default)</td> </tr> </tbody> </table>	X	<i>PULSE_SLOW</i>	<i>PULSE_FAST</i>	$1.5 * 2^2 = 6$	-1	-1	$1.5 * 2^6 = 96$	-1	1	$1.5 * 2^{-4} = 0.09375$	1	-1	1.5	1 (default)	1 (default)
X	<i>PULSE_SLOW</i>	<i>PULSE_FAST</i>																
$1.5 * 2^2 = 6$	-1	-1																
$1.5 * 2^6 = 96$	-1	1																
$1.5 * 2^{-4} = 0.09375$	1	-1																
1.5	1 (default)	1 (default)																
29	<i>PULSE_FAST</i>	1																
2D	<i>WRATE</i>	1556	$Kh = VMAX * IMAX * 47.1132 / (ln_8 * WRATE * N_{ACC} * X)$ Wh/pulse.															
37	<i>EXT_PULSE</i>	15	Should be 15 or 0. When zero, causes the pulse generators to respond to <i>WSUM_X</i> and <i>VARSUM_X</i> . Otherwise, the generators respond to values the host places in <i>APULSEW</i> and <i>APULSER</i> .															
3C	<i>PULSE_WIDTH</i>	50	The maximum pulse width (low-going pulse) is $(2 * PULSE_WIDTH + 1) * 397\mu s$. 0 is a legitimate value.															
26	<i>APULSEW</i>		Watt pulse generator input (see <i>DIO_PW</i> bit). The output pulse rate is: $APULSEW * F_S * 2^{-32} * WRATE * X * 2^{-14}$. This input is buffered and can be loaded during a computation interval and will take effect at the beginning of the next interval. Default value is 0.															
27	<i>APULSER</i>		VAR pulse generator input (see <i>DIO_PV</i> bit). The output pulse rate is: $APULSER * F_S * 2^{-32} * WRATE * X * 2^{-14}$. This input is buffered and can be loaded during a computation interval and will take effect at the beginning of the next interval. Default value is 0.															

WRATE controls the number of pulses that are generated per measured Wh and VARh quantities. The lower *WRATE* is the slower the pulse rate for measured power quantity. The metering constant *Kh* is derived from *WRATE* as the amount of energy measured for each pulse. That is, if *Kh* = 1Wh/pulse, a power applied to the meter of 120V and 30A results in one pulse per second. If the load is 240V at 150A, ten pulses per second will be generated.

Control is transferred to the MPU for pulse generation if *EXT_PULSE* > 0. In this case, the pulse rate is determined by *APULSEW* and *APULSER*. The MPU has to load the source for pulse generation in *APULSEW* and *APULSER* to generate pulses. Irrespective of the *EXT_PULSE* status the output pulse rate controlled by *APULSEW* and *APULSER* is implemented by the CE only. By setting *EXT_PULSE* > 0, the MPU is providing the source for pulse generation. If *EXT_PULSE* is negative, *WOSUM_X* and *VAROSUM_X* are the default pulse generation sources. In this case, creep cannot be controlled since it is an MPU function.

The maximum pulse rate is $F_s/2 = 1260.3\text{Hz}$.

PULSE_WIDTH allows adjustment of the pulse width for compatibility with calibration and other external equipment. The minimum pulse width possible is 397 μs .

The maximum time jitter is 397 μs and is independent of the number of pulses measured. Thus, if the pulse generator is monitored for 1 second, the peak jitter is 397ppm. After 10 seconds, the peak jitter is 40ppm. The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it will simply output at its maximum rate without exhibiting any roll-over characteristics. The actual pulse rate, using *WSUM* as an example, is:

$\text{RATE} = \text{WRATE} * \text{WSUM} * X / (2^{46} * T_{\text{MUX}})$, measured in Hz, where $T_{\text{MUX}} = \text{MUX frame period}$.

Current Shunt Variables

Input variables: *IA_SHUNT* and *IB_SHUNT* can configure the current inputs to accept shunt resistor sensors. In this case the CE provides an additional gain of 8 to the current inputs. This will enable the pulse rate to change by 8 times. In order to maintain a normal pulse rate *WRATE* may have to be decreased by 8 times. Whenever *IA_SHUNT* or *IB_SHUNT* are set to 1 or a positive number *I_n_8* (in the equation for *kh*) is assigned a value of 8.

CE Address	Name	Default	Description
2A	<i>IA_SHUNT</i>	-1	When +1, these variables increase the respective current gain by 8. The gain factor controlled by <i>IX_SHUNT</i> is referred to as <i>I_n_8</i> throughout this document. Allowed values are 1 or -1. For example, if <i>IB_SHUNT</i> = -1, <i>I₁_8</i> = 1, if <i>IB_SHUNT</i> = 1, <i>I₁_8</i> = 8. <i>IA_SHUNT</i> corresponds to <i>I₀_8</i> , <i>IB_SHUNT</i> corresponds to <i>I₁_8</i> .
2B	<i>IB_SHUNT</i>	-1	
2C	<i>RESERVED</i>		

CE Calibration Parameters

The table below lists the parameters that are typically entered to effect calibration of meter accuracy.

CE Address	Name	Default	Description
8	<i>CAL_IA</i>	16384	These constants control the gain of their respective channels. The nominal value for each parameters is $2^{14} = 16384$. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% slow, CAL should be scaled by $1/(1 - 0.01)$.
9	<i>CAL_VA</i>	16384	
A	<i>CAL_IB</i>	16384	
B	<i>RESERVED</i>		
C	<i>RESERVED</i>		
D	<i>RESERVED</i>		
E	<i>PHADJ_A</i>	0	These two constants control the CT phase compensation. No compensation occurs when $PHADJ_X = 0$. As $PHADJ_X$ is increased, more compensation (lag) is introduced. Range: $\pm 2^{15} - 1$. If it is desired to delay the current by the angle Φ : $PHADJ_X = 2^{20} \frac{0.02229 \cdot TAN\Phi}{0.1487 - 0.0131 \cdot TAN\Phi} \text{ at 60Hz}$
F	<i>PHADJ_B</i>	0	
10	<i>RESERVED</i>	0	

Other CE Parameters

The table below shows CE parameters used for suppression of noise due to scaling and truncation effects as well as scaling factors.

CE Address	Name	Default	Description
2F	<i>QUANT</i>	0	This parameter is added to the Watt calculation to compensate for input noise and truncation. $LSB = (VMAX \cdot IMAX / In_8) \cdot 7.4162 \cdot 10^{-10} \text{ W}$
34	<i>QUANT_VAR</i>	0	This parameter is added to the VAR calculation to compensate for input noise and truncation. $LSB = (VMAX \cdot IMAX / In_8) \cdot 7.4162 \cdot 10^{-10} \text{ W}$
35	<i>QUANT_I</i>	0	This parameter is added to compensate for input noise and truncation in the squaring calculations for I^2 and V^2 . $LSB = VMAX^2 \cdot 7.4162 \cdot 10^{-10} \text{ V}^2$ $LSB = (IMAX^2 / In_8^2) \cdot 7.4162 \cdot 10^{-10} \text{ A}^2$
3B	<i>KVAR</i>	6448	Scale factor for the VAR calculation. The default value of <i>KVAR</i> should never need to be changed.

ELECTRICAL SPECIFICATIONS
ABSOLUTE MAXIMUM RATINGS

Supplies and Ground Pins:	
V3P3D, V3P3A	-0.5V to 4.6V
VLCD	-0.5V to 7V
VBAT	-0.5V to 4.6V
GNDD	-0.5V to +0.5V
Analog Output Pins:	
VREF, VBIAS	-1mA to 1mA, -0.5V to V3P3A+0.5V
V2P5	-1mA to 1mA, -0.5V to 3.0V
Analog Input Pins:	
IA, VA, IB, V1	-0.5V to V3P3A+0.5V
XIN, XOUT	-0.5V to 3.0V
OPT_RX	-1mA to 1mA
All Other Pins:	
All other pins	-0.5V to V3P3D+0.5V
Operating junction temperature (peak, 100ms)	140 °C
Operating junction temperature (continuous)	125 °C
Storage temperature	-45 °C to 165 °C
Solder temperature – 10 second duration	250 °C

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

RECOMMENDED EXTERNAL COMPONENTS

NAME	FROM	TO	FUNCTION	VALUE	UNIT
C1	V3P3A	AGND	Bypass capacitor for 3.3V supply	≥0.1±20%	μF
C2	V3P3D	DGND	Bypass capacitor for 3.3V supply	≥0.1±20%	μF
XTAL	XIN	XOUT	32.768kHz crystal. Electrically similar to Ecliptek ECPSM310T series	32.768	kHz
CXS	XIN	AGND	Load capacitor for crystal (depends on crystal specs and board parasitics).	10±10%	PF
CXL	XOUT	AGND	Load capacitor for crystal (depends on crystal specs and board parasitics).	10±10%	PF
CBIAS	VBIAS	AGND	Bypass capacitor for VBIAS	≥1000±20%	PF
CBST1	VDRV	external	Boost charging capacitor	33±20%	NF
C2P5	V2P5	DGND	Bypass capacitor for V2P5	≥0.1±20%	μF
CBST2	VLCD	DGND	Boost bypass capacitor	≥0.22±20%	μF

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
3.3V Supply Voltage (V3P3A, V3P3D)	Normal Operation	3.0	3.3	3.6	V
	Battery Backup	0		3.45	V
Voltage difference V3P3A – V3P3D		-0.5		+0.5	V
VLCD		2.9		5.5	V
VBAT	No Battery	Externally Connect to V3P3D			
	Battery Backup	2.0		3.8	V
Operating Temperature		-40		85	°C

PERFORMANCE SPECIFICATIONS
LOGIC LEVELS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Digital high-level input voltage, V _{IH}		2		V3P3D	V
Digital low-level input voltage, V _{IL}		-0.3		+0.8	V
Digital high-level output voltage V _{OH}	I _{LOAD} = 1mA	V3P3D -0.4		V3P3D	V
	I _{LOAD} = 15mA	V3P3D -0.6			V
Digital low-level output voltage V _{OL}	I _{LOAD} = 1mA	0		0.4	V
	I _{LOAD} = 15mA			0.8	V
Input pull-up current, I _{IH} RESETZ E_RXTX, E_RST Other digital inputs	VIN=0V	10		100	μA
		10		100	μA
		-1		+1	μA
					μA
Input pull down current, I _{IH} TEST Other digital inputs	VIN=V3P3D	10		100	μA
		-1		+1	μA

COMPARATORS

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Offset Voltage V1-VBIAS		-20		15	mV
Hysteresis Current V1	Vin = VBIAS - 100mV	0.8		1.2	μA
Response Time V1	±100mV overdrive	2		15	μs
WD Disable Threshold (V1-V3P3A)		-400		-10	mV

SUPPLY CURRENT

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V3P3A + V3P3D + VLCD current	Normal Operation,		6.4	9.5	mA
V3P3A current	V3P3A=V3P3D=VLCD=3.3V		3.7	4.3	mA
V3P3D current	CKMPU=614kHz		2.5	4.8	mA
VLCD current	VBAT=3.6V		0.2	0.4	mA
VBAT current	No Flash memory write	-300		300	nA
V3P3A + V3P3D current	Power save/sleep mode V3P3A=V3P3D=VLCD=3.3V		6	7	mA
V3P3D current, Write Flash	Normal Operation as above, except write Flash at maximum rate.		7		mA
VBAT current, VBAT=3.6V	Battery backup, $\leq 25^{\circ}\text{C}$		2	4	μA
	V3P3A=V3P3D=VLCD=0V $f_{\text{osc}} = 32\text{kHz}$ 85°C		4	12	μA

VREF, VBIAS

 Unless otherwise specified, $V_{\text{REF_DIS}}=0$

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VREF output voltage, VNOM(25)	Ta = 22°C	1.193	1.195	1.197	V
VREF chop step				40	mV
VREF output impedance	CAL = 1, ILOAD = 10 μA , -10 μA			2.5	k Ω
VNOM definition ^A	$V_{\text{NOM}}(T) = V_{\text{REF}}(22) + (T-22)TC1 + (T-22)^2TC2$				V
-- If TRIMBGA and TRIMBGB available (6511H) --					
VREF temperature coefficients TC1 TC2 TRIMBGA, TRIMBGB, TRIMM[2:0]: See TRIMSEL, TRIM registers	$x(33-0.28y) + 0.33y + 7.9$ $x(0.02-0.0002y) - 0.46$ where $x = 0.1\text{TRIMBGB} + 0.14(\text{TRIMM}[2:0]+0.5)$, $y = (\text{TEMP_NOM} - 500\text{TRIMBGA} - 370,000)/900$				$\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/^{\circ}\text{C}^2$
VREF(T) deviation from VNOM(T) $\frac{V_{\text{REF}}(T) - V_{\text{NOM}}(T)}{V_{\text{NOM}}} \frac{10^6}{\max(T - 22 , 40)}$		-10		10	ppm/ $^{\circ}\text{C}$
-- If TRIMBGA and TRIMBGB not available (6511) --					
VREF temperature coefficients TC1 TC2			-6.68 -0.341		$\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/^{\circ}\text{C}^2$
VREF(T) deviation from VNOM(T) $\frac{V_{\text{REF}}(T) - V_{\text{NOM}}(T)}{V_{\text{NOM}}} \frac{10^6}{\max(T - 22 , 40)}$	Ta = -40°C to +85°C	-40		+40	ppm/ $^{\circ}\text{C}$
VBIAS output voltage	Ta = 25°C	(-1%)	1.5	(+1%)	V
	Ta = -40°C to 85°C	(-2%)	1.5	(+2%)	V
VBIAS output impedance	ILOAD = 1mA, -1mA		240	500	Ω

^A This relationship describes the nominal behavior of VREF at different temperatures.

2.5V VOLTAGE REGULATOR

Unless otherwise specified, load = 5mA

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage overhead V3P3-V2P5	Reduce V3P3 until V2P5 drops 200mV			440	mV
PSSR $\Delta V2P5/\Delta V3P3$	RESETZ=1, iload=0	-3		+3	mV/V

ADC CONVERTER, VDD REFERENCED

FIR_LEN=0, VREF_DIS=0, VDDREFZ=0

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Recommended Input Range (Vin-V3P3A)		-250		250	mV peak
Voltage to Current Crosstalk: $\frac{10^6 * V_{crosstalk}}{V_{in}} \cos(\angle V_{in} - \angle V_{crosstalk})$	<i>Vin</i> = 200mV peak, 65Hz, on VA <i>Vcrosstalk</i> = largest measurement on IA or IB	-10		10	μ V/V
THD (First 10 harmonics) 250mV-pk 20mV-pk	<i>Vin</i> =65Hz, 64kpts FFT, Blackman- Harris window			-75 -90	dB dB
Input Impedance	<i>Vin</i> =65Hz	60		90	k Ω
Temperature coefficient of Input Impedance	<i>Vin</i> =65Hz		1.7		$\Omega/^\circ$ C
LSB size			355		nV/LSB
Digital Full Scale			+884736		LSB
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \Delta N_{out_{pk}} 357nV / V_{IN}}{100 \Delta V3P3A / 3.3}$	<i>Vin</i> =200mV pk, 65Hz V3P3A=3.0V, 3.6V			50	ppm/ %
Input Offset (Vin-V3P3A)		-10		10	mV

CRYSTAL OSCILLATOR

 Crystal is disconnected. Test load is series 200pF, 100k Ω connected between DGND and XOUT.

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Maximum Output Power to Crystal ⁴	Crystal connected			1	μ W
Xin to Xout Capacitance ¹				3	pF
Capacitance to DGND ¹ Xin Xout				5 5	pF pF
Watchdog RTC_OK threshold				25	kHz

OPTICAL INTERFACE

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
OPT_TX V _{OH} (V3P3D-OPT_TX)	I _{SOURCE} =1mA			0.4	V
OPT_TX V _{OL}	I _{SINK} =20mA			0.7	V
OPT_RX Vin Threshold (V _{inRISING} +V _{inFALLING})/2		200	250	300	mV
OPT_RX Vin Hysteresis (V _{inRISING} -V _{inFALLING})		5		30	mV
OPT_RX input impedance	V _{in} ≤300mV	1			MΩ

TEMPERATURE SENSOR

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Nominal Sensitivity (S _n) ⁴	T _A =25°C, T _A =75°C		-900		LSB/°C
Nominal Offset (N _n) ⁴	Nominal relationship: N(T)= S _n *T+N _n		400000		LSB
Temperature Error ¹ $ERR = (T - 25) - \frac{(N(T) - N(25))}{S_n}$	T _A = -40°C to +85°C	-3		3	°C

LCD BOOST

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VDRV Frequency			OSC/2		Hz
VDRV Sink Current	V _{ol} =1.5V	1.2		2.75	mA
VDRV Source Current	V _{oh} =1.5V	1.2		2.6	mA
VLCD Target Voltage		4.5		5.5	V
VLCD Input Current	VLCD=5.0V, LCD_FS=1F, LCD_MODE=0,1,2,3			450	μA

LCD DRIVERS

Applies to all COM and SEG pins. Unless otherwise stated, VLCD=5.0V, LCD_FS=1F

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VLC0 Max Voltage (LCD_FS =1F)	With respect to VLCD	-0.2		0	V
VLC0 Min Voltage (LCD_FS =00)	With respect to VLCD*0.7	-0.2		0.2	V

RTC

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Range for date		2000	-	2255	year

TIMING SPECIFICATIONS
RAM AND FLASH MEMORY

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
CE RAM wait states	CKMPSU = 4.9MHz	5			Cycles
	CKMPSU = 1.25MHz	2			Cycles
Flash write cycles		20,000			Cycles
Flash data retention	25°C	100			Years

FLASH MEMORY TIMING

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Write Time per Byte			42		µs
Page Erase (512 bytes)			20		ms
Mass Erase			200		ms

EEPROM INTERFACE

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Write Clock frequency	CKMPSU=4.9MHz, Using interrupts		78		kHz
	CKMPSU=4.9MHz, "bit- banging" DIO4/5		150		kHz

RESETZ

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Reset pulse width		5			µs
Reset pulse fall time				1	µs

FOOTNOTES

- ¹This spec is guaranteed, has been verified in production samples, but is not measured in production.
- ²This spec is guaranteed, has been verified in production samples, but is measured in production only at DC.
- ³This spec is measured in production at the limits of the specified operating temperature.
- ⁴This spec defines a nominal relationship rather than a measured parameter. Correct circuit operation is verified with other specs that use this nominal relationship as a reference.

TYPICAL PERFORMANCE DATA

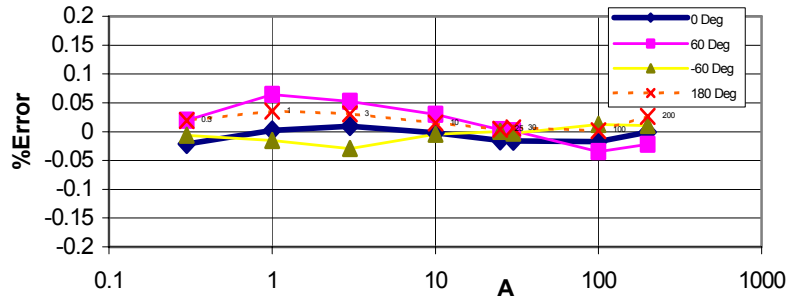


Figure 9: Wh Accuracy, 0.3A - 200A/240V

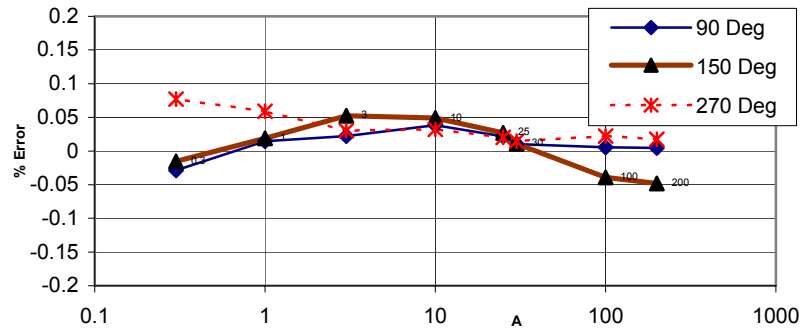
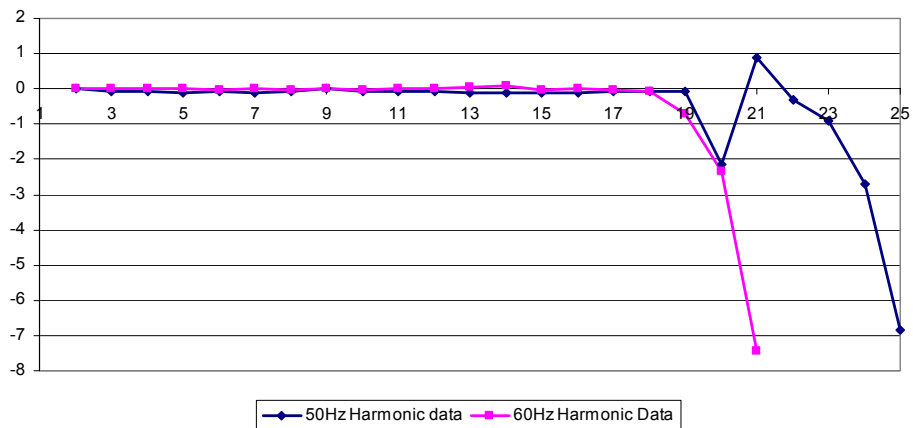


Figure 10: VARh Accuracy for 0.3A to 200A/240V Performance



Measured at current distortion amplitude of 40% and voltage distortion amplitude of 10%.

Figure 11: Meter Accuracy over Harmonics at 240V, 30A

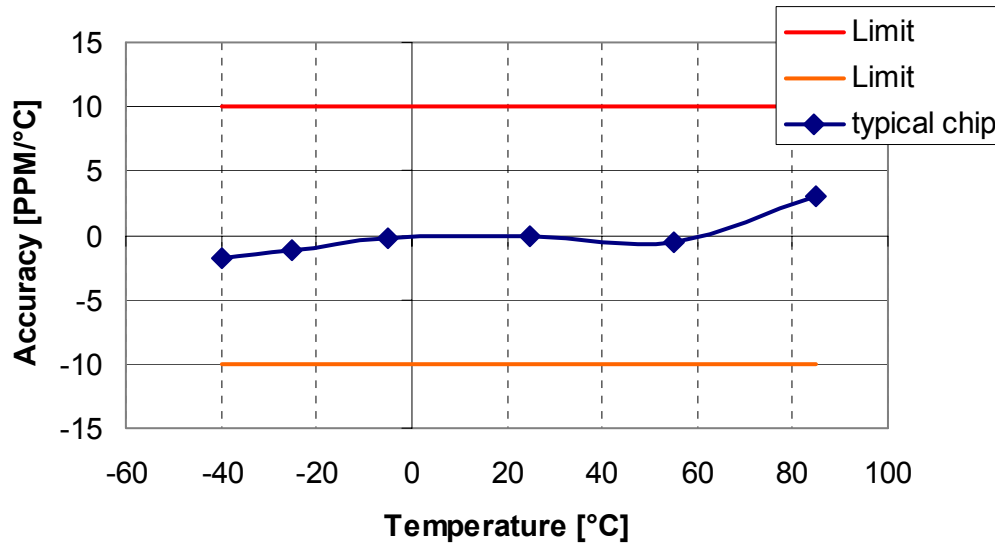
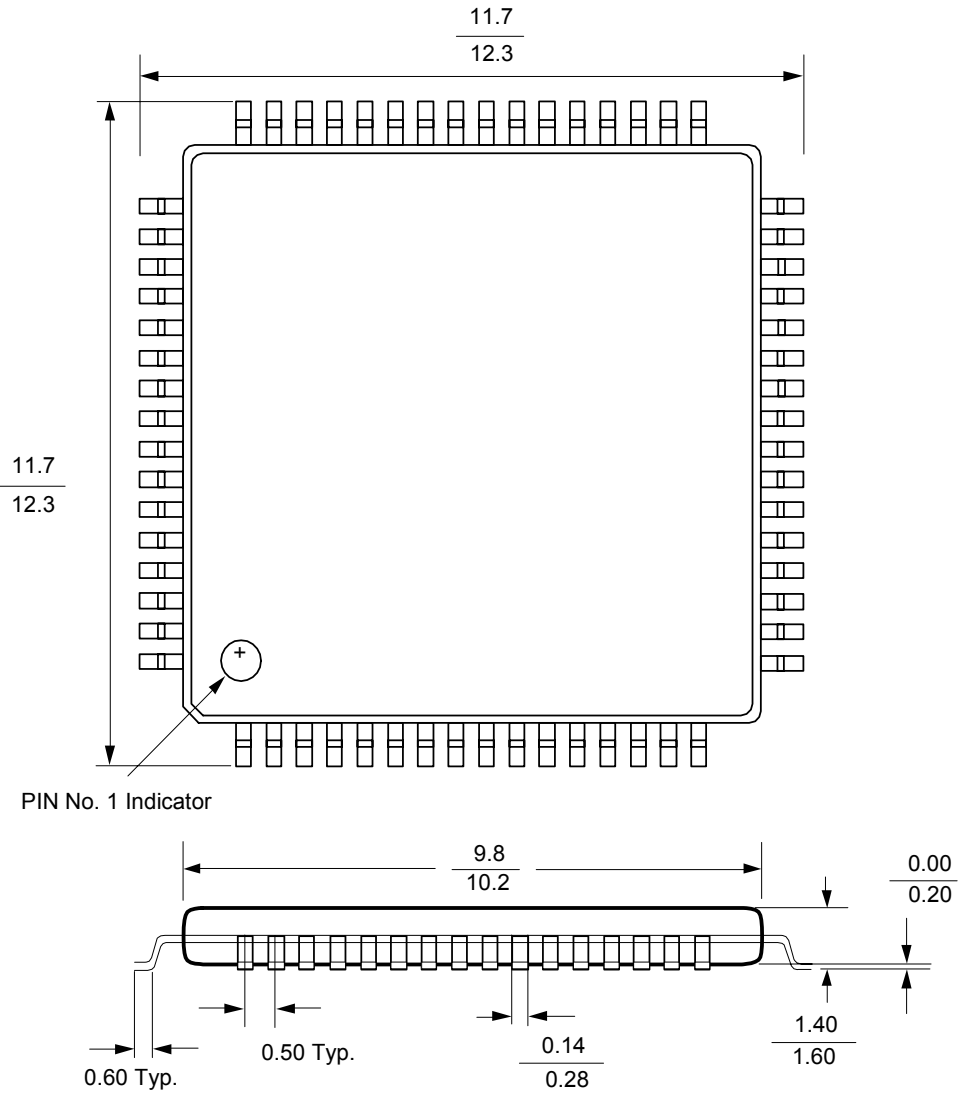


Figure 12: Typical Meter Accuracy over Temperature Relative to 25°C (w/ Temperature Compensation)

PACKAGE OUTLINE

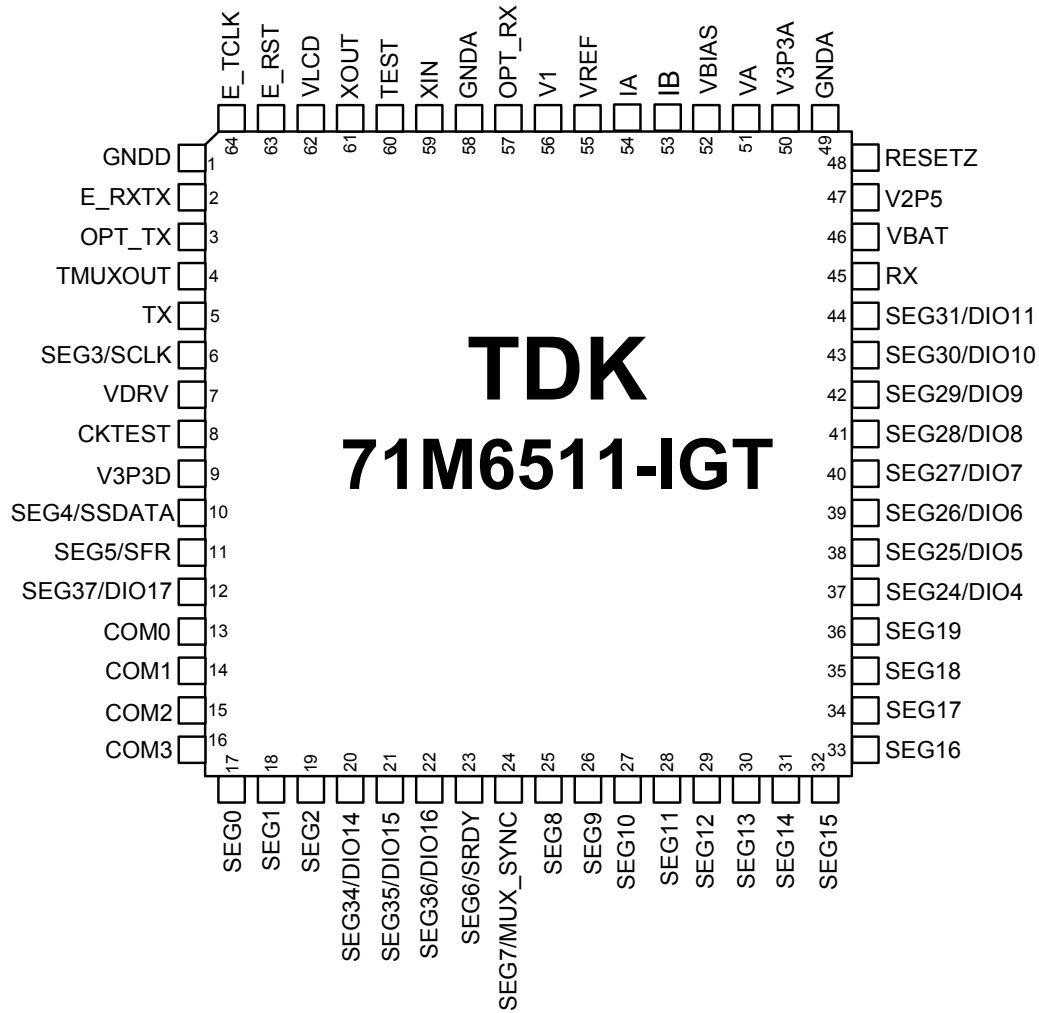


NOTE: CONTROLLING DIMENSIONS ARE IN mm

DATASHEET

MARCH 2005

PINOUT:



PIN DESCRIPTIONS
Power/Ground Pins:

Name	Pin #	Type	Description
GNDA	49, 58	P	Analog ground: This pin should be connected directly to the ground plane.
GNDD	1	P	Digital ground: This pin should be connected directly to the ground plane.
V3P3A	50	P	Analog power supply: A 3.3V power supply should be connected to this pin.
V3P3D	9	P	Digital power supply: A 3.3V power supply should be connected to this pin.
VBAT	46	P	Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3D.
V2P5	47	O	Output of the internal 2.5V regulator. A 0.1 μ F capacitor to GNDA should be connected to this pin.
VLCD	62	P	LCD power supply.

Analog Pins:

Name	Pin #	Type	Description
IA	54	I	Line Current Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a current transformer.
VA	51	I	Line Voltage Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a resistor divider.
IB	53	I	Line Current Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a current transformer.
V1	56	I	Comparator Input: This pin is a voltage input to the internal comparator. The voltage applied to the pin is compared to an internal reference voltage of 1.5V. If the input voltage is above the reference, the comparator output will be high (1). If the comparator output is low, a voltage fault will occur. A 0.1 μ F capacitor to GNDA should be connected to this pin.
VREF	55	O	Voltage Reference for the ADC. A 0.1 μ F capacitor to GNDA should be connected to this pin.
VBIAS	52	O	The reference voltage used by the power fault detection circuit.
XIN XOUT	59 61	I	Crystal Inputs: A 32kHz style crystal should be connected across these pins. Typically, a 10pF capacitor is also connected from each pin to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details.
VDRV	7	O	Voltage boost output.

Digital Pins:

Name	Pin #	Type	Description
COM3, COM2, COM1, COM0	16 15 14 13	O	LCD Common Outputs: These 4 pins provide the select signals for the LCD display.
SEG19...SEG8, SEG2...SEG0	See pinout	O	Dedicated LCD Segment Output.
SEG24/DIO4... SEG31/DIO11, SEG34/DIO14... SEG37/DIO17	See pinout	O	Multi-use pin, configurable as either LCD SEG driver or DIO. (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface, WPULSE = DIO6, VARPULSE = DIO7 when configured as pulse outputs)
SEG7/ MUX_SYNC	24	O	Multi-use-pin LCD Segment Output/ MUX_SYNC is output for Synchronous serial interface
SEG6/SRDY	23	I/O	Multi-use-pin, LCD Segment Outputs/ SRDY input for Synchronous serial interface.
SEG5/SFR	11	O	Multi-use-pin, LCD Segment Output/ SFR output for Synchronous serial interface.
SEG4/SDATA	10	O	Multi-use-pin, LCD Segment Output/ SDATA output for Synchronous serial interface.
SEG3/SCLK	6	O	Multi-use-pin, LCD Segment Output/ SCLK output for Synchronous serial interface.
CKTEST	8	O	Clock PLL output. Can be enabled and disabled by <i>CKOUT_EN</i> .
TMUXOUT	4	O	Digital output test multiplexer. Controlled by <i>DMUX[3:0]</i> .
OPT_RX	57	I	Optical Receive Input: This pin receives a signal from an external photo-detector used in an IR serial interface.
OPT_TX	3	O	Optical LED Transmit Output: This pin is designed to directly drive an LED for transmitting data in an IR serial interface. Can be tristated with <i>OPT_TXDIS</i> to be multiplexed with other DIO pins.
RESETZ	48	I	Chip reset: This input pin is used to reset the chip into a known state. For normal operation, this pin is set to 1. To reset the chip, this pin is driven to 0. This pin has an internal 30 μ A (nominal) current source pull up. A 0.1 μ F capacitor to GNDD should be connected to this pin.
RX	45	I	UART input.
TX	5	O	UART output.
E_RXTX	2	I/O	Emulator serial data. This pin has an internal pull-up resistor.
E_TCLK	64	O	Emulator clock. This pin has an internal pull-up resistor.
E_RST	63	I	Emulator reset. This pin has an internal pull-up resistor.
TEST	60	I	Enables Production Test. Must be grounded in normal operation.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING
71M6511 64 pin LQFP, 0.5% accuracy	71M6511-IGT	71M6511-IGT
71M6511 64 pin LQFP Lead Free, 0.5% accuracy	71M6511-IGT/F	71M6511-IGT
71M6511H 64 pin LQFP, 0.1% accuracy	71M6511H-IGT	71M6511H-IGT
71M6511H 64 pin LQFP Lead Free, 0.1% accuracy	71M6511H-IGT/F	71M6511H-IGT

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