Power-over-Ethernet Interface PD Controller Demo Board

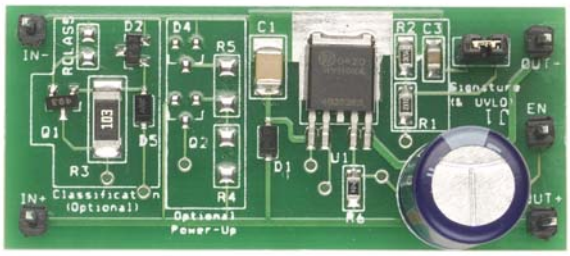
Introduction

The Supertex HV110DB2 demo board is a complete power management and protection solution for Powered Devices (PDs) utilizing the IEEE802.3af protocol. The HV110 features a 400mA inrush limit and fault current limit, as well as minimum current shutdown to ensure additional protection to expensive equipment connected to the PD switch. The HV110DB2 is configured to operate in Class 0. Other classes can easily be implemented by soldering one resistor on the board (see Classification Section). The HV110 has passed the IOL (*Inter Operability Lab*) tests for a PD controller.

The demo board can be used to test the performance of the HV110 as a power management and protection device for the downstream power supply. The input voltage source is connected between IN+ and IN– and the external load is connected between OUT+ and OUT–. The input capacitor of the DC/DC stage, which is usually present, is already included on the demo board as capacitor C2.

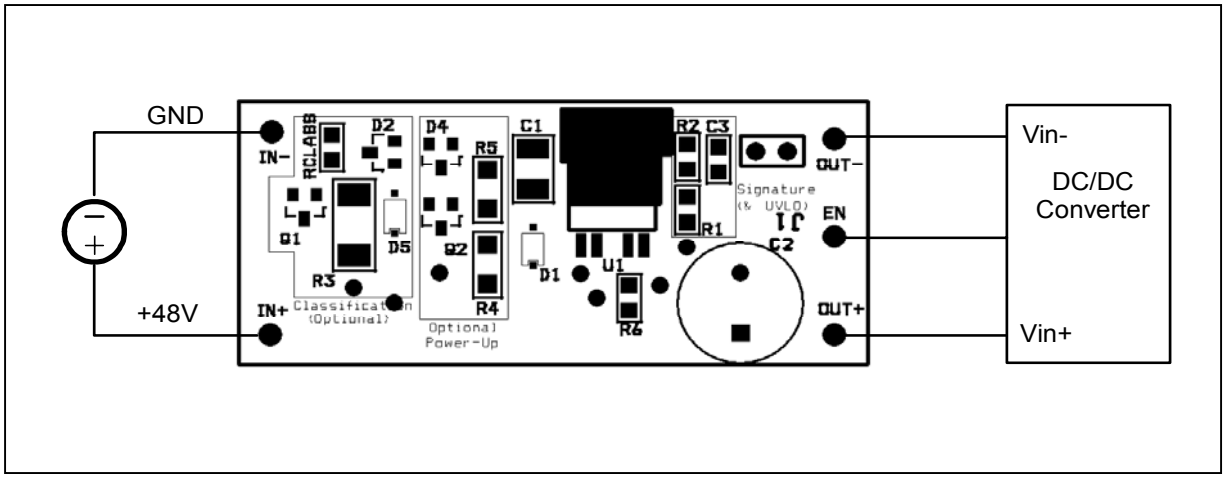
Specifications

Input	0 - 57V (V_{pp} referenced to V_{nn})
Load Current	350mA
Load Current Limit	400mA (max)
Undercurrent limit	5mA
R_{ds} of the internal FET	1Ω (at Ids = 200mA)
UVLO	Turn on at 40V Turn off at 32V



Board Dimensions: 50.9mm x 22.3mm

Schematic Diagram



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Instructions

IN+ : Connect the positive of the supply voltage to this terminal.

IN- : Connect the negative of the supply voltage.

OUT+: Connect the positive terminal of the output DC/DC converter (or active load) to this terminal.

OUT-: Connect the negative terminal of the output DC/DC converter (or active load) to this terminal.

EN: This terminal can be used as an enable signal for the external DC/DC converter. The signal is active low and behaves as high impedance during inrush and short circuit. Resistor R3 on the board is used to pull the signal up to V+ during inrush limit and short circuit. The pull-up resistor R3 has to be chosen carefully. The $\overline{PWRGD}$ output pin of the HV110 has a rated pull-up current of 3mA and a maximum leakage current (in the high impedance state) of 10μA. Using a very small pull-up resistor will cause a large current in the low state damaging the internal FET. Using a very large R3 will cause a large voltage drop across it due to the leakage current causing the voltage at the pin to drop to very small levels and behaving like active LOW.

Notes:
An external DC/DC converter can be connected between OUT+ and OUT- to verify the performance of the HV110. The DC/DC converter can be enabled using the EN terminal of the HV110DB2.

The EN terminal will be at +48V with respect to OUT- during the start-up and short-circuit conditions. This high voltage might damage the DC/DC converter. Before connecting the EN pin to the Enable input of the DC/DC converter, make sure that the voltage levels are compatible (external circuit at the EN pin might be necessary).

The 0.47μF capacitor (C1) at the V_{pp} pin of the HV110 does not violate the IEEE specifications during the *Discovery* Process (which limit the total capacitance seen to 0.1μF). The voltage applied during the *Discovery* process is about 2.8V – 10V and the 10V zener (D1) will block the 0.47μF capacitor during this time.

The resistance of the external circuit connected between the OUT+ and OUT- terminals of the HV110DB2 should be greater than 500k (in the 2.8V – 10V Discovery voltage range) for the signature detect to work properly.

Programming the UVLO

The undervoltage turn-on and turn-off voltages can be programmed by changing resistors R1 and R2. However, the sum of the two resistors has to be about 25kΩ since these resistors also participate in the *Discovery Process.* The resistors used on the HV110DB2 set the turn-on threshold at 40V and the turn-off threshold at 32V.

Testing the HV110DB2

Apply a differential 48V between the IN+ and IN- pins, while introducing some contact bounce. Notice that the voltage on the output capacitor ramps up neatly after the contact bounce has been cleared. The EN pin will go to low once the load capacitor C2 has been charged up to the input voltage.

During the same test, monitor the input current by means of a small current sense resistor or a current probe. The input inrush current will be limited to 350mA (nom) during start-up.

Apply a short circuit on the output by shorting OUT+ to OUT-. The HV110 will limit the short circuit current at 400mA (max). If the fault is not cleared within a nominal 60ms, the HV110 will turn-off and initiate an auto-restart routine.

Check the under voltage lockout by reducing the input voltage to 30V. The HV110 shuts down and will restart only when the voltage goes above 40V.

Remove the load on the HV110DB2 to test the undercurrent timer. The HV110 shuts off after 350ms and the EN signal goes high.

Note that the HV110 incorporates some of the timing functions of a PSE. Thus, it acts as a backup in case the PSE fails and protects the PD.

PNP Power-up *(optional)*

In the HV110DB2, a 10V zener diode (D1) is connected between IN+ and the Vpp pin of the HV110. This zener diode blocks the HV110 during the Discovery stage. However, the zener reduces the voltage seen by the HV110 at its V_{pp} pin. Thus, the built in hysteresis can no longer be used. In order to use the built-in input undervoltage hysteresis,

- diode D1 has to be removed
- PNP power-up circuit has to be assembled (see Schematic and Bill of Materials)
- Shunt on connecter J1 has to removed
- Resistor R3 has to be changed to a 120k, 1/4W resistor

This circuit ensures the HV110 does not draw any current in the Discovery stage. However, once the input voltage exceeds 12V, zener D4 turns on providing base current to transistor Q2. This base current causes Q2 to saturate raising the voltage at the V_{pp} pin of the HV110 to the input voltage. In this case, the UVLO pin can be left open.

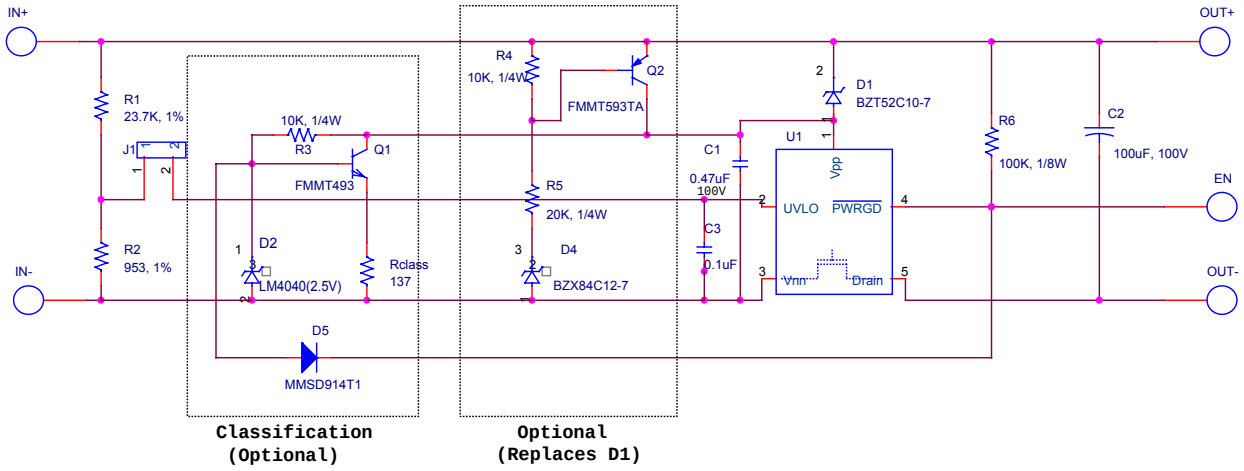
Classification Circuit

The external classification circuit can be used to program the Class of the PD. The classification is set by changing one resistor – R_{class}. The classification resistor is set according to the table below.

Class	R_{class}
0	Open
1	210 ohm, 1/10W, 1% SMD 0805
2	107 ohm, 1/10W, 1% SMD 0805
3	71.5 ohm, 1/10W, 1% SMD 0805

Note: *In all cases, the HV110 will be preceded by a diode bridge rectifier (as required by the IEEE802.3af), and the classification voltage will be measured at the input to the diode bridge. The classification resistors given in the table assume the presence of the diode bridge. Measuring the classification current without the diode bridge may cause the circuit to fall out of the IEEE802.3af specification for classification currents.*

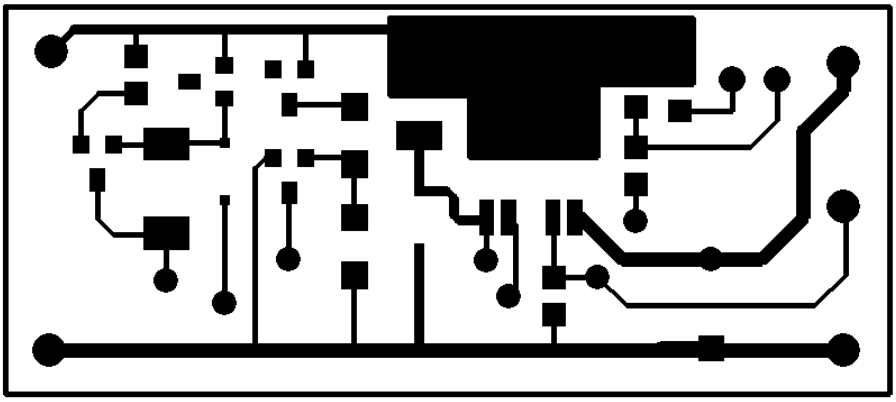
HV110DB2 - Schematic



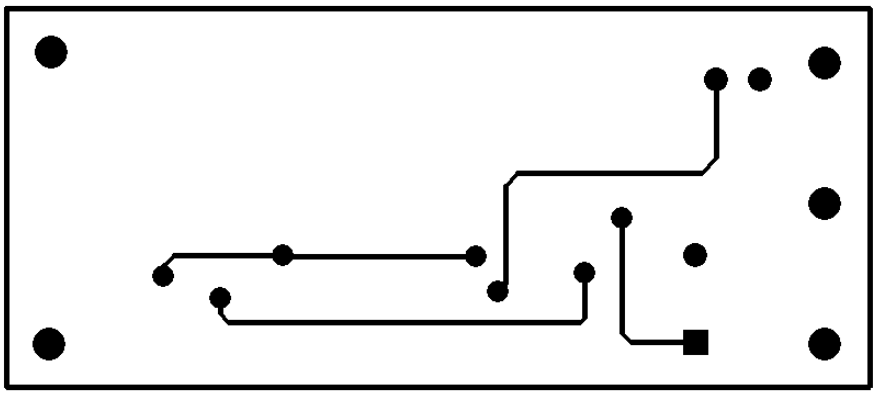
HV110DB2 – Bill of Materials

Quantity	RefDes	Description	Package	Manufacturer	Manufacturer's Part Number
1	C1	0.47uF, 100V ceramic capacitor	SMD1210	Panasonic	ECJ-4YB2A474K
1	C2	100uF, 100V Electrolytic capacitor		Panasonic	ECA-2AM101
1	C3	0.1uF, 25V ceramic capacitor	SMD0805	Panasonic	ECJ-2VF1E104Z
1	D1	10V, 500mW zener diode	SOD-123	Diodes, Inc.	BZT52C10-7
5	OUT-,OUT+,IN-,IN+,EN	5 Position Breakaway Header		Molex/ Waldom	22-28-4050
1	J1	2 pin header, 2mm pitch		Sullins	PRPN021PAEN
1	R1	23.7K, 1%, 1/4W chip resistor	SMD1206	Yageo	9C12063A2372FKHFT
1	R2	953, 1%, 1/10W chip resistor	SMD0805	Panasonic	ERJ-6ENF9530V
1	R6	100K, 5%, 1/8W chip resistor	SMD0805	Panasonic	ERJ-6GEYJ104V
1	U1	PD controller	DPAK-5	Supertex	HV110
Classification Circuit					
1	Q1	100V, 500mA NPN transistor	SOT-23	Zetex	FMMT614TA
1	D2	2.5V, 1%, fixed voltage reference	SOT-23	Zetex	ZRC250F01TA
1	*Rclass*	*1%, 1/10W resistor*	*SMD0805*		*See demoboard datasheet for values*
1	R3	10K, 5%, 1/4W chip resistor	SMD1206	Panasonic	ERJ-8GEYJ103V
Optional Power-up circuit					
1	D4	12V, 350mW zener diode	SOT-23	Diodes, Inc.	BZX84C12-7
1	Q2	-100V, -1A PNP transistor	SOT-23	Zetex	FMMT593TA
1	*R3*	*120K, 5%, 1/4W chip resistor*	*SMD1206*	*Panasonic*	*ERJ-8GEYJ124V (use instead of 10K)*
1	R4	2K, 5%, 1/4W chip resistor	SMD1206	Panasonic	ERJ-8GEYJ202V
1	R5	3.9K, 5%, 1/4W chip resistor	SMD1206	Panasonic	ERJ-8GEYJ392V

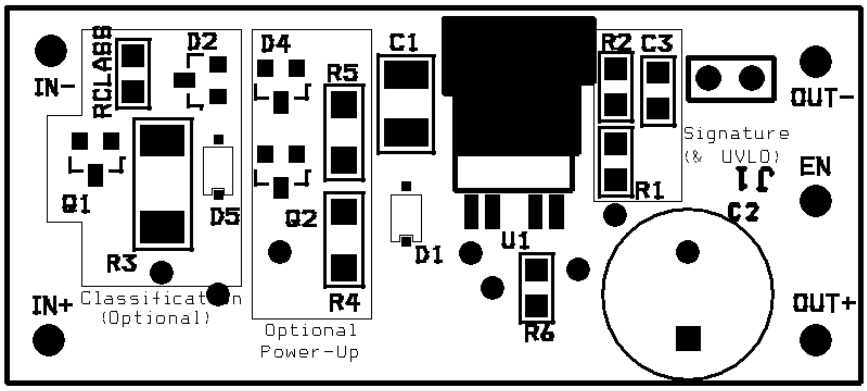
HV110DB2 – Top View



HV110DB2 – Bottom View



HV110DB – Top Silk Layer



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