



## Power-over-Ethernet Interface PD Controller meets IEEE 802.3af™ Standards

**OBSOLETE**

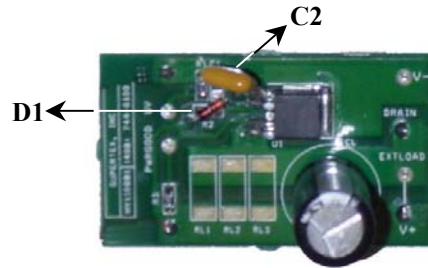
### Introduction

The Supertex HV110DB1 demo board is a complete power management and protection solution for Powered Devices (PDs) utilizing the IEEE802.3af protocol. HV110 features a 400mA inrush limit and fault current limit, as well as minimum current shutdown to ensure additional protection to expensive equipment connected to the PD switch. The HV110DB1 is intended to be used for Class 0 applications and does not provide any classification functions. The HV110DB1 has passed the IOL (*Inter Operability Lab*) tests for a PD controller.

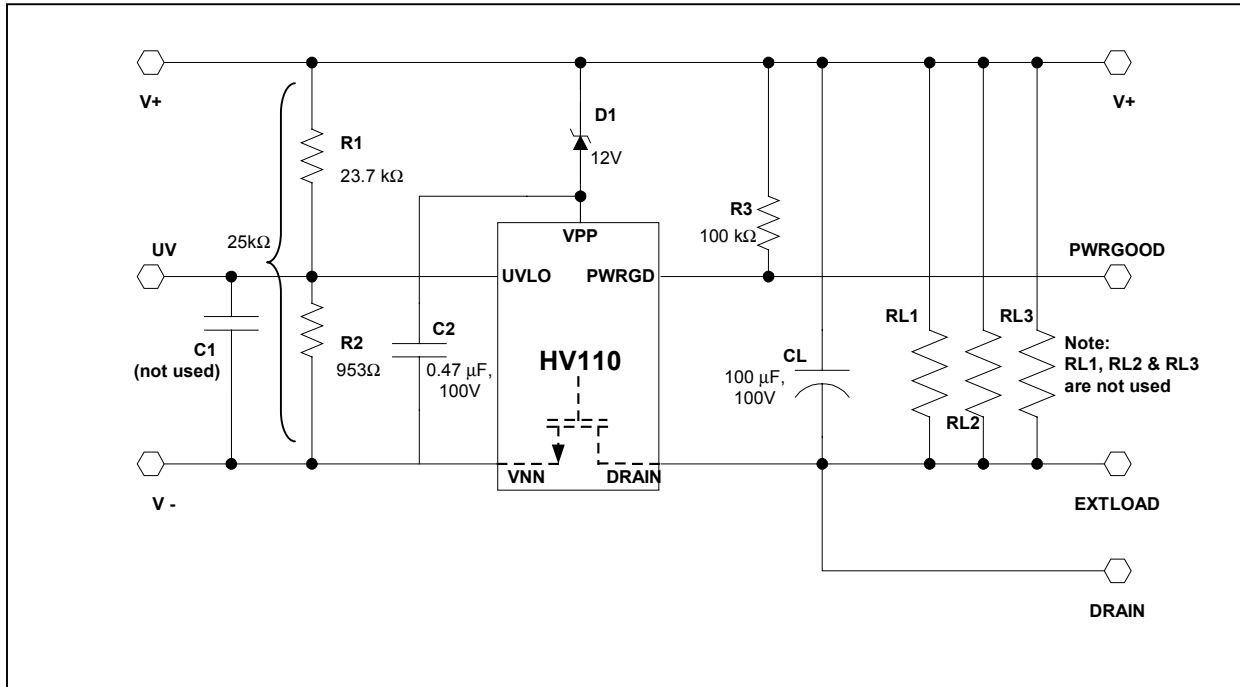
The demo board can be used to test the performance of the HV110 as a power management and protection device for the downstream PD. The input voltage source is connected between V+ and V- and the external load is connected between V+ and EXTLOAD. The input capacitor of the DC/DC stage, which is usually present, is already included on the demo board as capacitor CL.

### Specifications

|                                     |   |
|-------------------------------------|---|
| Input                               | 0 - 57V<br>(V <sub>pp</sub> referenced to V <sub>nn</sub> ) |
| Load Current                        | 300mA nominal   |
| Load Current Limit                  | 350mA   |
| Undercurrent limit                  | 10mA  |
| R <sub>ds</sub> of the internal FET | 1Ω (at I <sub>ds</sub> = 200mA)                             |
| UVLO                                | Turn on at 40V<br>Turn off at 32V                           |



### Schematic Diagram



## Instructions

**V+** : Connect the positive of the supply voltage to this terminal. The positive of the load is also to be connected to the same terminal.

**V-** : Connect the negative of the supply voltage.

**EXTLOAD (also DRAIN)**: These two terminals are connected on the board. The negative of the load is to be connected to this terminal.

**PWRGOOD** : This terminal can be used as an enable signal for the external DC/DC converter. The signal is active low and behaves as a high impedance during inrush and short circuit. Resistor R3 on the board is used to pull the signal up to V+ during inrush limit and short circuit. The pull-up resistor R3 has to be chosen carefully. The PWRGD output pin of the HV110 has a rated pull-up current of 3mA and a maximum leakage current (in the high impedance state) of 10 $\mu$ A. Using a very small pull-up resistor will cause a large current in the low state damaging the internal FET. Using a very large R3 will cause a large voltage drop across it due to the leakage current causing the voltage at the pin to drop to very small levels and behaving like active LOW.

Classification can be implemented by adding a few components as shown in the datasheet.

The resistance of the external circuit connected between the DRAIN and V+ terminals of the HV110DB1 should be greater than 500k (in the 2.8V – 10V Discovery voltage range) for the signature detect to work properly.

**UV** : This terminal is used to monitor the under voltage lockout setting for the HV110. The UVLO is set by the resistor divider formed by R1 and R2. Please refer to the HV110 datasheet for details on programming the UVLO threshold.

### Notes:

An external DC/DC converter can be connected between V+ and EXTLOAD to verify the performance of the HV110. The DC/DC converter can be enabled using the PWRGOOD terminal of the HV110DB1.

The 0.47 $\mu$ F capacitor at the V<sub>pp</sub> pin of the HV110 does not violate the IEEE specifications during the *Discovery Process* (which limit the total capacitance seen to 0.1 $\mu$ F). The voltage

applied during the *Discovery process* is about 2.8V – 10V and the 12V zener will block the 0.47 $\mu$ F capacitor during this time.

Through-hole parts D1 and C2 can be replaced by smaller surface mount components like the MMSZ12T1 (SOD123 package) and ECJ-4YB2A474K (SMD1210 package) respectively.

## Programming the UVLO

The undervoltage turn-on and turn-off voltages can be programmed by changing resistors R1 and R2. However, the sum of the two resistors has to be about 25k $\Omega$  since these resistors also participate in the *Discovery Process*.

## Testing HV110DB1

Apply a differential 48V between the V+ and V- pins, while introducing some contact bounce. Notice that the voltage on the output capacitor ramps up neatly after the contact bounce has been cleared. The PWRGOOD pin will go to low once the load capacitor CL1 has been charged up to the input voltage.

During the same test, monitor the input current by means of a small current sense resistor or a current probe. The input inrush current will be limited to 400mA during start-up.

Apply a short circuit on the output by shorting V+ to EXTLOAD. The HV110 will limit the short circuit current at 400mA. If the fault is not cleared within a nominal 60ms, the HV110 will turn-off and initiate an auto-restart routine.

Check the under voltage lockout by reducing the input voltage to 30V. The HV110 shuts down and will restart only when the voltage goes above 40V.

Remove the load on the HV110DB1 to test the undercurrent timer. The HV110 shuts off after 350ms and the PWRGOOD signal goes high.

Note that the HV110 incorporates some of the timing functions of a PSE. Thus, it acts as a backup in case the PSE fails and protects the PD.