

## 1.0. Kit Contents

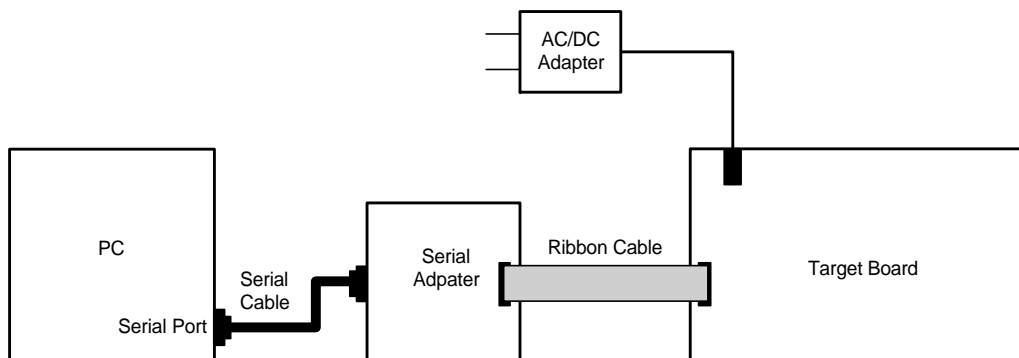
The C8051F30X Development Kit contains the following items:

- C8051F30X Target Board
- Serial Adapter (RS-232 to Target Board Protocol Converter)
- Cygnal IDE and Product Information CD-ROM. CD content includes:
  - Cygnal Integrated Development Environment (IDE)
  - Keil Software 8051 Development Tools (macro assembler, linker, evaluation 'C' compiler)
  - Installation utility (SETUP.EXE)
  - Source code examples and register definition file
  - Documentation
- AC to DC Power Adapter
- RS232 Serial Cable
- 7" Ribbon Cable
- Quick-start Guide
- C8051F30X Development Kit User's Guide (this document)

## 2.0 Hardware Setup

The target board is connected to a PC running the Cygnal IDE via the Serial Adapter as shown in Figure 1.

1. Connect one end of the RS232 serial cable to a serial (COM) port on the PC.
2. Connect the other end of the RS232 serial cable to the DB-9 connector on the Serial Adapter.
3. Connect the Serial Adapter to the DEBUG connector on the target board using the 10-pin ribbon cable.
4. Connect the AC/DC power adapter to power jack P1 on the target board.



**Figure 1. Hardware Setup**

**Note:** The Reset switch on the target board is disabled when the Serial Adapter is connected to the target board. Use the **Reset** button in the Cygnal IDE toolbar to reset the target when connected to the Serial Adapter.

## 3.0. Software Setup

The included CD-ROM contains the Cygnal Integrated Development Environment (IDE), Keil Software 8051 tools and additional documentation. Insert the CD-ROM into your PC's CD-ROM drive. An installer will automatically launch allowing you to install the IDE software or read documentation by clicking buttons on the Installation Panel. (If the installer does not automatically start when you insert the CD-ROM, run "autorun.exe" found in the root directory of the CD-ROM.) Refer to the "README.TXT" file on the CD-ROM for the latest information regarding IDE known problems and restrictions.

**Note:** C8051F30X family devices use the Cygnal 2-wire (C2) debug interface. You must select **Cygnal 2-wire (C2)** in the **Options->Debug Interface** menu of the Cygnal IDE to enable connection to 'F30X target devices.

## 4.0. CYGNAL Integrated Development Environment

The included CD-ROM contains the Cygnal Integrated Development Environment (IDE). The Cygnal IDE integrates a source-code editor, source-level debugger and in-system Flash programmer. The use of third-party compilers and assemblers is also supported. This development kit includes the Keil Software A51 macro assembler, linker and evaluation version C51 'C' compiler which can be used from within the Cygnal IDE.

### 4.1. System Requirements

The Cygnal IDE requires:

- Pentium-class host PC running Microsoft Windows 95/98, Windows NT or Windows 2000.
- One available COM port (1-4).
- 64MB RAM and 40MB free HD space recommended.

### 4.2. Assembler and Linker

A full-version Keil A51 macro assembler and BL51 banking linker are included with the development kit and are installed during IDE installation. The complete assembler and linker reference manual can be found on-line under the **Help** menu in the IDE or in the "Cygnal\hlp" directory (A51.PDF).

### 4.3. Evaluation C51 'C' Compiler

An evaluation version of the Keil C51 'C' compiler is included with the development kit and is installed during IDE installation. The evaluation version of the C51 compiler is the same as the full professional version except code size is limited to 4K bytes and the floating point library is not included. The C51 compiler reference manuals can be found in the "Cygnal\hlp" directory (C51.PDF).

### 4.4. Using the Keil Software 8051 Tools with the Cygnal IDE

To perform source-level debug with the IDE, you must configure the Keil 8051 tools to generate an absolute object file in the OMF-51 format with object extensions and debug records enabled. You may build the OMF-51 absolute object file by calling the Keil 8051 tools at the command line (e.g. batch file or make file) or by using the project manager built into the IDE. The default configuration when using the Cygnal IDE project manager enables object extension and debug record generation.

To build an absolute object file using the Cygnal IDE project manager, you must first create a project. A project consists of a set of files, IDE configuration, debug views, and a target build configuration (list of files and tool configurations used as input to the assembler, compiler, and linker when building an output object file).

The following sequence illustrates the steps necessary to manually create a project with one or more source files, build a program and download the program to the target in preparation for debugging. (The IDE will automatically create a single-file project using the currently open and active source file if you select **Build or Make Project** before a project is defined.) Refer to Applications Note AN004 in the “*Documentation*” directory on the CD-ROM for additional information on using the Keil 8051 tools with the Cygnal IDE.

#### 4.4.1. Creating a New Project

1. Select **File -> New File** to open an editor window. Create your source file(s) and save the file(s). (Color syntax highlighting will be enabled once the file is saved with a recognized extension such as .c, .h or .asm.)
2. Right-click on “New Project” in the **Project Window**. Select **Add files to project**. Select a file to add to the project in the file browser and click Open.
3. Select the **File Group** to which you want to add the file(s) and click **Add Group**. Repeat steps 2 and 3 for each file you want to add to the project.
4. For each of the files in the **Project Window** that you want assembled, compiled and linked into the target build, right-click on the file name and select **Add file to build**. Each file will be assembled or compiled as appropriate (based on file extension) and linked into the build of the absolute object file.

#### 4.4.2. Building and Downloading the Program for Debugging

1. Once all source files have been added to the target build, click on the **Build** button in the toolbar (or select **Project -> Build/Make Project** to build and download the program to the target hardware for debug.

By default, if the program build is successful, the IDE will automatically connect to the target and download the program for debug. (This may be disabled by deselecting **Enable automatic connect/download after build** in the **Projects -> Target Build Configuration** dialog.) If errors occur during the build process, the IDE will not attempt the download.

2. Save the project when finished with the debug session to preserve the current target build configuration, editor settings and the location of all open debug views. To save the project, right-click on the **New Project** entry in the **Project Window** and select **Save as a project**.

### 4.5. Example Source Code

Example source code and register-definition files are installed into the “*Examples\C8051F3XX*” directory during IDE installation. The source files may be used as a template for F30X code development. The *C8051F3XX.INC* and *c8051f3xx.h* files define the addresses for all F30X SFR registers and bit-addressable control/status bits. The register and bit names are identical to those used in the C8051F30X datasheet. Both register definition files are also installed in the default search path used by the Keil Software 8051 tools. Therefore, when using the Keil 8051 tools (A51, C51) it is not necessary to copy a register definition file to each project's file directory.

## 5.0. Target Board

The C8051F30X Development Kit includes a target board with a C8051F30X device pre-installed for evaluation and preliminary software development. Numerous input/output (I/O) connections are provided to facilitate prototyping using the target board. Refer to Figure 2 for the locations of the various I/O connectors. Table 1 shows the pin-out of the J1 connector.

- P1 - Power connector (accepts input from 7 to 15 VDC unregulated power adapter)
- J1 - 12-pin Expansion I/O connector
- J3 - Port I/O Configuration Jumper Block
- J5 - DB9 connector for UART0 RS232 interface
- J6 - Analog I/O terminal block
- DEBUG - Used to connect the Serial Adapter to the target board via a 10-pin ribbon cable

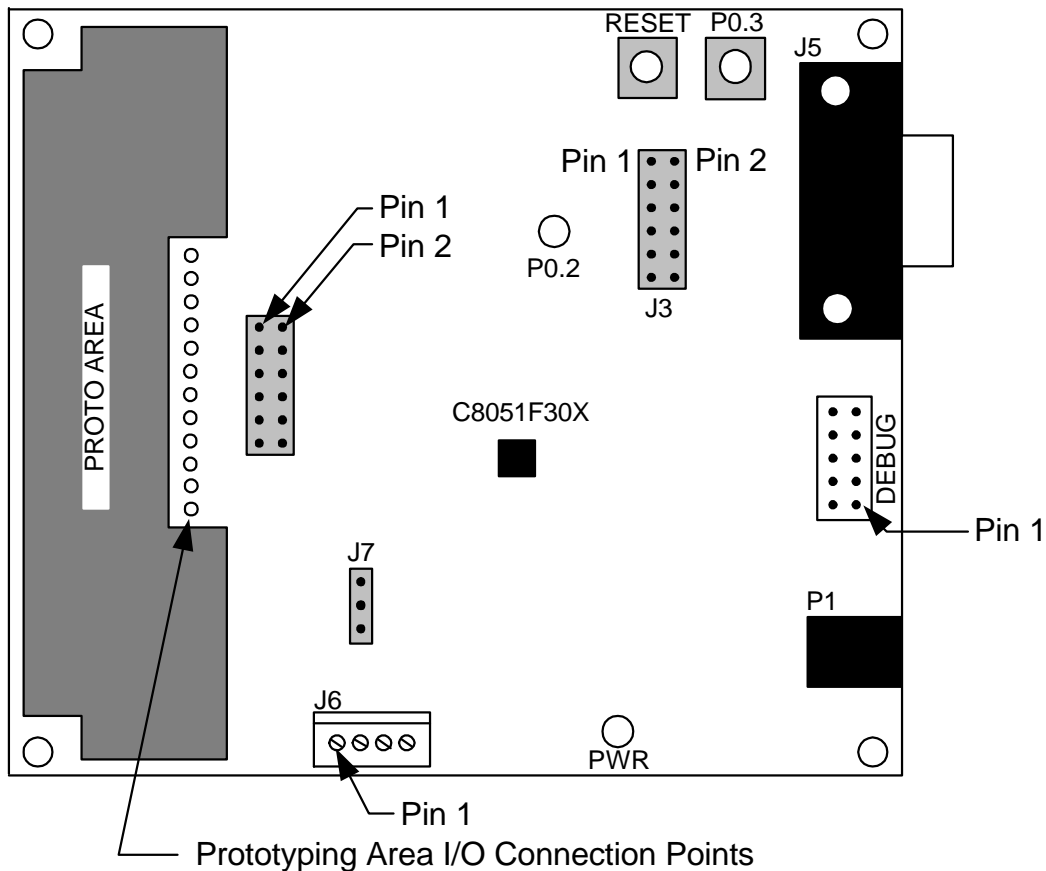


Figure 2. C8051F30X Target Board

## 5.1. System Clock Sources

The C8051F30X device installed on the target board features a calibrated programmable internal oscillator which is enabled as the system clock source on reset. After reset, the internal oscillator operates at a frequency of 3.0625MHz (+/-2%) by default but may be configured by software to operate at other frequencies. Therefore, in many applications an external oscillator is not required. However, if you wish to operate the C8051F30X device at a frequency not available with the internal oscillator, an external crystal may be used.

The target board is designed to facilitate the installation of an external crystal at the pads marked Y1. To use an external crystal, remove resistors R7 and R8 and install the crystal at the pads labeled Y1. Install a 10M resistor at R9 and install capacitors at C14 and C15 using values appropriate for the crystal you select. Refer to the C8051F30X datasheet for more information on the configuration of the programmable internal oscillator and the use of external oscillators.

## 5.2. Switches and LEDs

Two switches and two LEDs are provided on the target board. Switch SW1 is connected to the RESET pin of the C8051F30X. Pressing SW1 puts the C8051F30X in its hardware-reset state. Switch SW2 is connected to the C8051F30X's Port 0.3 (P0.3) general purpose I/O (GPIO) pin. Pressing SW2 generates a logic low signal on the P0.3 pin. Remove the shorting block from J3[3-4] to disconnect SW2 from P0.3.

The LED labeled PWR is used to indicate a power connection to the target board. The LED labeled P0.2 is connected to the C8051F30X's Port 0.2 (P0.2) GPIO pin through jumper J3[1-2]. The P0.2 signal is also routed to a pin on the J1 I/O connector. Remove the shorting block from J3[1-2] to disconnect the LED from P0.2.

## 5.3. Expansion I/O Connector (J1)

The 12-pin Expansion I/O connector J1 provides access to all signal pins of the C8051F30X device. Pins for +3V, digital ground and the output of an on-board low-pass filter also available. A small through-hole prototyping area is also provided. All I/O signals routed to connector J1 are also routed to through-hole connection points between J1 and the prototyping area (see Figure 2). Each connection point is labeled indicating the signal available at the connection point.

Pin	Description
1	+3VD (+3.3VDC)
2	PWM Output
3	P0.0
4	P0.1
5	P0.2
6	P0.3
7	P0.4
8	P0.5
9	P0.6
10	P0.7
11	GND (Ground)
12	/RST (Reset)

**Table 1. J1 Pin Descriptions**

## 5.4. Serial Interface (J5)

An RS232 transceiver circuit and DB-9 (J5) connector are provided on the target board to facilitate serial connections to UART0 of the C8051F30X. The TX and RX signals of UART0 may be connected to the DB9 connector and transceiver by installing jumpers on J3.

- J3[5-6] - Install shorting block to connect UART0 TX (P0.4) to transceiver.
- J3[7-8] - Install shorting block to connect UART0 RX (P0.5) to transceiver.

## 5.5. Analog I/O (J6)

Several of the C8051F30X target device's port pins which can be used for analog inputs are connected to the J20 terminal block. Refer to Table 2 for the J20 terminal block connections. Install a shorting block on J7[2-3] to connect the AIN6 input to the P0.6 pin of the target device.

Pin	Description
1	P0.1/AIN1 (ADC Input 1)
2	AIN6 (ADC Input 6)
3	GND (Ground)
4	P0.0/Vref (Voltage Reference)

**Table 2. J6 Terminal Block**

## 5.6. Low-pass Filter (J7)

The target board features a low-pass filter that may be connected to port pin P0.6. Install a shorting block on J7[1-2] to connect the P0.6 pin of the target device to the low-pass filter input. The output of the low-pass filter is routed to the PWM signal at J1[2]. The C8051F30X may be programmed to generate a PWM (Pulse-Width Modulated) waveform which is then input to the low-pass filter to implement a user-controlled PWM digital-to-analog converter. Refer to Applications Note AN007 in the "Documentation" directory on the CD-ROM for a discussion on generating a programmable DC voltage level with a PWM waveform and low-pass filter.

## 5.7. Target Board DEBUG Interface (J4)

The DEBUG connector (J4) provides access to the DEBUG pins of the C8051F30X. It is used to connect the Serial Adapter to the target board for in-circuit debug and Flash programming. Table 3 shows the J4 pin definitions.

Pin	Description
1	2.7 to 3.6VDC Input
2, 3, 9	Ground
4	C2D (C2DAT)
5	/RST
6	P0.7
7	C2CK (C2CLK)
8, 10	Not Connected

**Table 3. DEBUG Connector Pin Descriptions**

## 6.0. Serial Adapter

The Serial Adapter provides the interface between the PC's RS232 serial port and the C8051F30X's in-system debug/programming circuitry. The EC2 Serial Adapter connects to the C8051F30X 2-wire C2 debug interface on the target board using the 10-pin connector on the Serial Adapter labeled "JTAG". (The EC2 Serial Adapter supports both Cygnal JTAG and C2 debug interfaces.). The Serial Adapter may be powered from the target board via the Serial Adapter's 10-pin ribbon cable or it may be powered directly from the included AC/DC power adapter. (The target board can not be powered from the Serial Adapter.) Figure 3 shows the pin definitions for the Serial Adapter's JTAG connector.

Notes:

1. When powering the Serial Adapter via the JTAG connector, the input voltage to the JTAG connector's power pin must be 3.0 to 3.6VDC. Otherwise, the Serial Adapter must be powered directly by connecting the AC/DC adapter to the Serial Adapter's DC power jack.
2. The Serial Adapter requires a target system clock of 32Khz or greater.

Pin	Description
1	3.0 to 3.6VDC Input
2	Ground
4	TCK (C2DAT)
5	TMS
6	TDO
7	TDI (C2CLK)
3,8,9,10	Not Connected

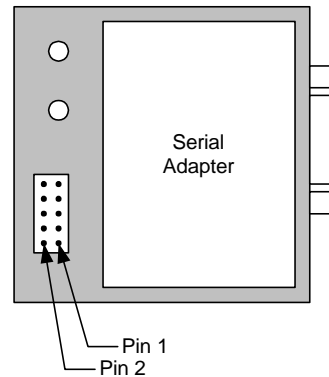


Figure 3. Serial Adapter JTAG Connector

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