

# eCOG1k Microcontroller

## Low Power Communications Processor

The eCOG1k microcontroller is a low-power microcontroller based on a 16-bit Harvard architecture with a 24-bit linear code address space (32Mbyte) and 16-bit linear data address space (128Kbytes). It is available in a 128-pin LQFP package. CyanIDE™, the industry leading toolset with automatic peripheral configuration and an ANSI C Compiler, is free of charge. A comprehensive Development Kit is available.

- ◆ 0 to 25MHz 3.3V processor
- ◆ Powerful arithmetic operations
- ◆ Barrel Shifter
- ◆ Harvard Architecture
- ◆ 64Kx16 Data Memory Space
- ◆ 16Mx16 Code Memory Space
- ◆ Built in Emulator (eICE)
- ◆ Low power operation
- ◆ 64Kbytes FLASH EPROM
- ◆ 4Kbytes SRAM
- ◆ MMU
- ◆ Power-saving code cache
- ◆ Code security feature
- ◆ External Host Interface
- ◆ External Memory Interface
- ◆ Fast Vectored Interrupts
- ◆ Dual UART
- ◆ Dual USART
- ◆ Smart Card Interface
- ◆ SPI
- ◆ I<sup>2</sup>C
- ◆ Infra-Red link support
- ◆ 4 channel 12-bit ADC
- ◆ Parallel Interface
- ◆ 5 Multi Purpose Timers
- ◆ Watchdog Timer
- ◆ Long Interval Timer
- ◆ Clock Timer
- ◆ PWM timers
- ◆ Temperature Sensor
- ◆ Supply Voltage Sensor
- ◆ Power-On Reset
- ◆ 88 Digital I/O pins
- ◆ 29 General Purpose I/O pins
- ◆ 25MHz from watch crystal
- ◆ Interfaces to 8/16/32-bit parts

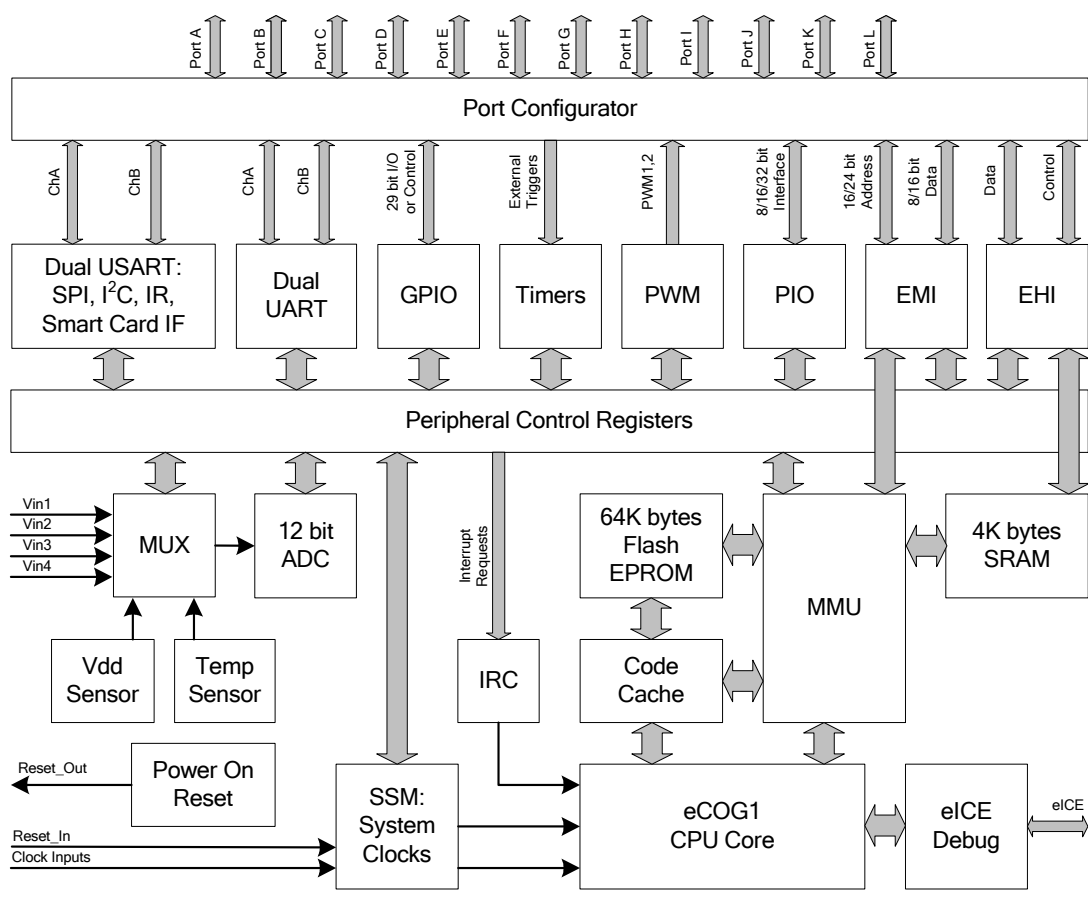


Figure 1 – Internal Block Diagram

**CPU Core**

- 16-bit 25MHz accumulator-based core
- Harvard architecture
- Supports a full array of 16-bit arithmetic operations, including both signed and unsigned MULTiply and DIVide instructions
- 32MByte linear program memory
- 128KByte linear data memory
- Vectored interrupts

**Flash EPROM**

- 64Kbytes organized as 32Kx16
- Organized as eight 4Kx16 banks
- Individual Flash banks can be read and/or write protected
- Programming algorithm is available under application software control
- 200k write/erase cycles (typical)  
100 years data retention

**Code Cache**

- 512 line cache
- Reduces power consumption while improving performance
- Both deterministic and non-deterministic modes
- Individual cache lines can be locked
- Can cache both User and Interrupt Mode

**MMU**

- Performs logical to physical address translations
- Translates between RAM, Program Memory and external memory devices for both code and data accesses concurrently
- Lookup tables in RAM or Flash can be mapped between each memory area
- Up to 2 concurrent translations to external devices from code addresses
- Up to 3 concurrent translations to external devices from data addresses
- Wait states automatically generated
- Concurrent accesses to same device are prioritized
- Translations are prioritized to allow overlapped translations

**DUART**

- Two independent RS232 compatible asynchronous double-buffered serial ports

- Full modem support (CTS, RTS, DSR, DTR, DCD, and RI)
- Supports 5, 6, 7, or 8 bits of data
- 1, 1.5, or 2 stop bits
- Even, odd or no parity
- Automatic end-of-frame guard time insertion of 0 to 64 bit periods
- Receive timeout detection 0 to 64 bit periods
- Software Line Break generation
- Programmable Baud rate generator
- Interrupts generated on full and empty
- Receiver error detection for false start bits, parity errors and frame errors
- Configurable data polarity
- Oversampling of received data for noise immunity

**DUSART**

- Two synchronous/asynchronous double-buffered serial ports
- Programmable baud rate generator
- End of frame guard time insertion of 0 to 64 bit periods
- Receive timeout detection 0 to 64 bit periods
- Receiver error detection for false start bits, parity errors, frame errors and buffer overflow
- Configurable data and clock polarity
- Configurable data packing, MSB or LSB first
- Oversampling of received data for noise immunity

**Asynchronous Interface:**

- Asynchronous frames supporting 5, 6, 7, or 8 bits of data
- 1, 1.5, or 2 stop bits
- Even, odd or no parity
- Full modem support (CTS, RTS, DSR, DTR, DCD, and RI)
- Software Line Break generation

**Synchronous Interface:**

- Internal or external transmit and receive clock
- Full or half duplex
- Frame sizes from 1 to 16 bits with larger frames possible
- Support for NRZ, RZ
- PM, PWM and ASK modulation if used in conjunction with PWM timer

**User Serial Port (USR)**

- Provides direct access to internal registers of each USART
- Custom serial protocols may be emulated
- Up to 255 symbols per frame
- Parity may be automatically inserted or tested at the end of each frame
- Start bit edge detection
- Tx/Rx interrupts

**SPI**

- Master or slave SPI port
- Slave select signal
- Programmable clock polarity and clock/data phase

**Smart Card Interface**

- ISO 7816 compatible smart card interface
- Multiprocessor support
- Byte level support for T=0 and T=1 transmission protocols
- Detection and generation of the transmission error signal for T=0 protocol
- Automatic retransmission of corrupted bytes for T=0 protocol
- Independent controls for power and ground switching
- Hardware state machine for power up, reset and shutdown sequences

**Infra-Red Link**

- Programmable baud rates
- Support for low rate (<115.2 kbps) IrDA framing and modulation
- Compatible with common ASK, PM, PPM (e.g. RC-5) modulation schemes
- Variable frame lengths up to 255 bits
- Variable length multi-byte frames
- Half duplex operation supported using an integral transceiver frame duration (maximum 1023 symbols) to separate transmit and receive exchanges
- Raw IR mode (software modem) supported
- Programmable start, stop, data length, frame length and polarities
- Programmable start and stop sequences
- Support for current and future frame formats
- Carrier frequency generation

**I<sup>2</sup>C**

- Two wire I<sup>2</sup>C compatible port
- Address matching
- ACK bit and wait state insertion
- Multi-master arbitration
- Supports 10-bit addressing and fast mode

**External Host Interface (EHI)**

- Provides an interface to an external host processor or FIFO
- Supports both DMA and memory mapped peripheral modes
- Interrupt generated upon transfer

**DMA mode:**

- Supports master and slave mode timings
- 16/32-bit data bus
- Request & Acknowledge control lines
- Configurable master mode timing
- DMA connection into internal SRAM (11-bit block address, max 256 byte block size)
- Internal DMA controller supports circular and linked list buffer models

**Memory mapped mode:**

- Selectable block size  
256 x 16-bit data  
8 x 32-bit data
- Three control lines: chip select, read/write direction and wait
- Configurable control line senses

**General Purpose I/O (GPIO)**

- 29 memory mapped GPIO pins
- Configured individually as input, output, or bidirectional
- Normal or open drain outputs
- Direct drive LEDs
- Each input can generate an interrupt

**External Interrupts**

- Any GPIO configured as an input can generate an interrupt
- Level or edge sensitive interrupts

**Parallel Interface (PIO)**

- Two 8/16-bit parallel data ports
- Normal, open drain, or tri-state outputs

**Timers**

- 16-bit Watchdog Timer
- 16-bit Clock Timer
- 24-bit Long Interval Timer
- Two 16-bit PWM Timers
- Two 16-bit General Purpose Timers or Event Counters
- 16-bit Capture Timer with multiple event capture registers

**External Memory Interface**

- 8 or 16-bit data bus
- 16 or 24-bit address bus
- Multiplexed address/data for 16-bit data bus
- External memory devices can be mapped into both code and data space
- Supports SRAM (bus) and SDRAM interface modes
- Supports up to 128Mbyte single data rate 16-bit wide SDRAMs
- Four row/column SDRAM address multiplexing schemes
- Supports SDRAM auto and self refresh
- Configurable timing
- Supports low power SDRAM suspend/standby modes
- Single cycle data space access, code space burst access in conjunction with Code Cache
- Hardware support for software initialization and refresh of SDRAM

**Analogue Functions**

- 12-bit ADC with 8kHz sampling, differential input
- On-chip temperature sensor
- On-chip Power Supply Monitor
- 4 channel analogue multiplexer with four input modes:
  - i) Four channel inputs to the ADC for single ended use, using internal voltage reference
  - ii) Three channel inputs to the ADC, one input as external reference
  - iii) Three channel inputs to the ADC, one port as output of the internal reference voltage
  - iv) Two differential inputs

**Clocks**

- Two crystal oscillators
- Internal PLL
- Low cost 32kHz watch crystal can generate 25MHz internal clock
- Second oscillator uses a 5MHz crystal to generate 25MHz internal clock with low jitter

**C Compiler suite**

- ANSI C Compiler
- Validated to ANSI/ISO/FIPS-160
- ANSI Standard Library
- Macro Assembler
- Software Simulator and debugger

**eICE Debugger Interface**

- Real-time debug port
- Can program internal Flash
- When BRK command is locked in the cache, can provide virtually unlimited address breakpoints
- Commands include Reset, Stop, Run, Run to Break
- Non-intrusive read and write to any core register, including PC
- Read and write of any memory location

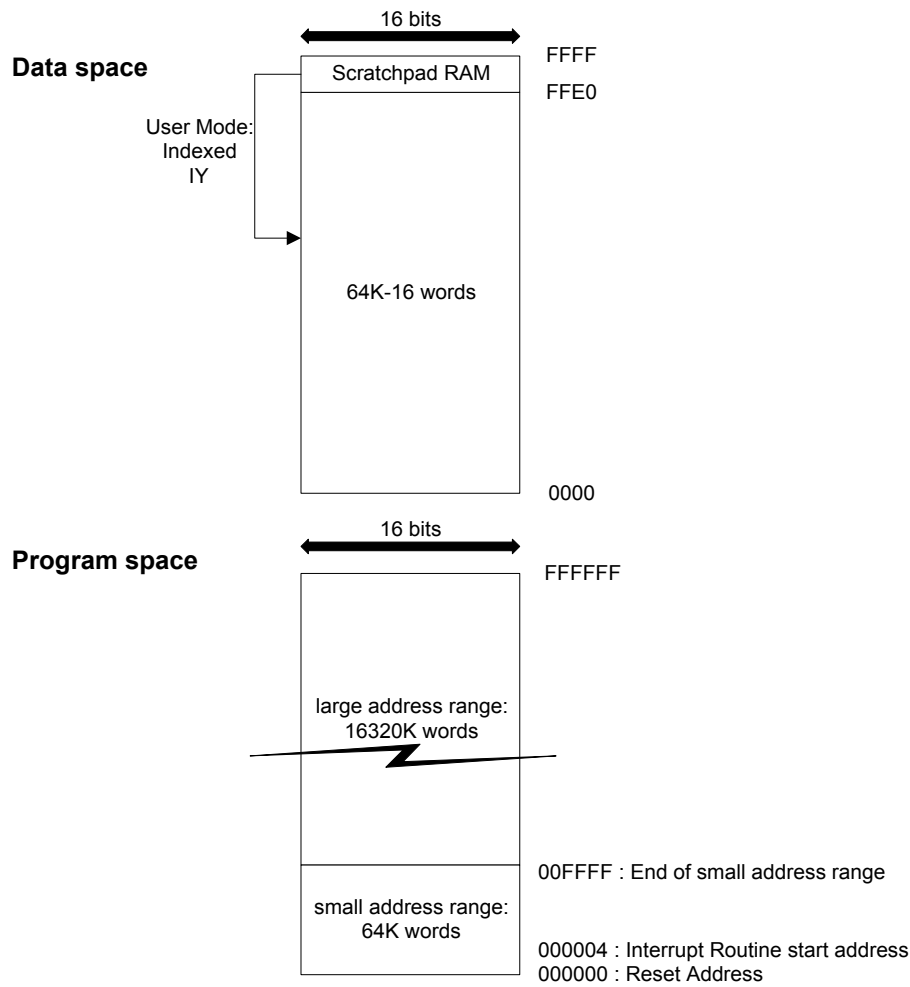
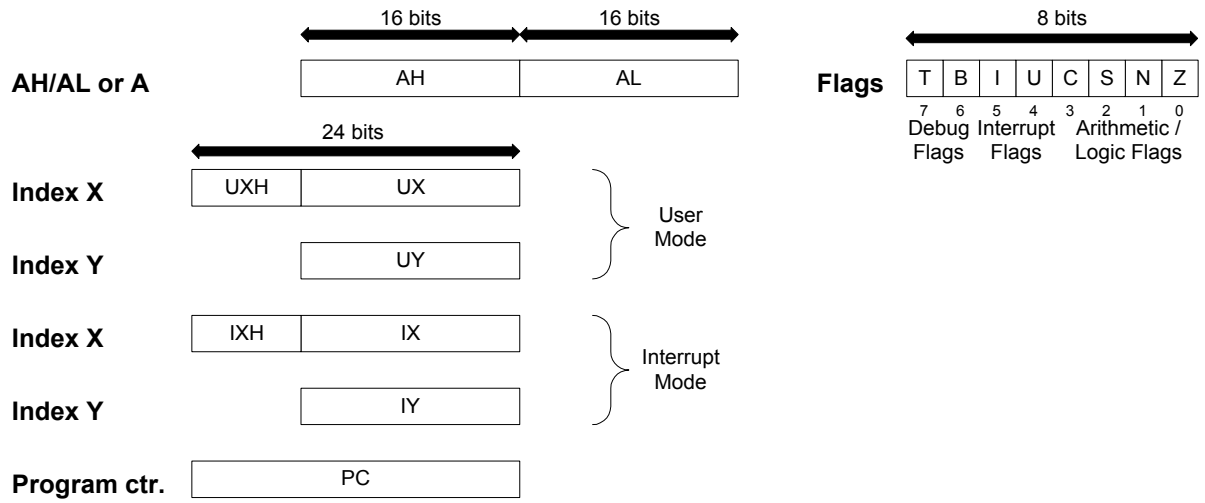
**Power Saving Features**

- Sleep mode with wake on interrupts
- All peripherals have individual clock domains and can be stopped when not in use

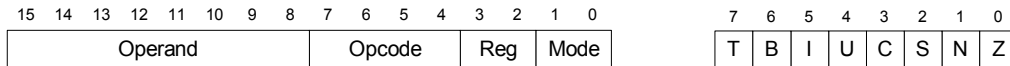
**External Ports**

- Peripherals are connected to multiple device pins
- Each port has a unique multiplexing scheme to select port configuration
- Ten 8-bit ports
- Two 4-bit ports

### Programmer's Model



## Instruction Set



Operand	Opcode	Reg	Mode	Assembler		Operation	Flags
not H'00	H'0	00	00	PREFIX	operand	ARG_EXT = (ARG_EXT<<8) + operand	-
H'00	H'0	00	00	NOP		None	-
H'00	H'0	01	00	BRK		Stop for debug	-
H'00	H'0	10	00	SLEEP		Enter sleep mode	-
H'00	H'0	11	00	SIF		Perform ESIF access during instruction	-
-	H'0	00	01	ST flags	@(<nn>,y)	@(<nn>,y) ← flags	-
-	H'0	01	01	LD flags	@(<nn>,y)	flags ← @(<nn>,y)	ALL
-	H'0	11	01	RTI	@(<nn>,y)	PC ← {IXH, IX}; flags ← data	ALL
H'00	H'0	10	01	UNSIGNED		Operation modifier: unsigned	-
H'01	H'0	10	01	SIGNED		-	-
H'FF	H'0	10	01	BC		for(AL; AL>0; AL--) @(<Y++>) ← @(<X++>)	-
H'FE	H'0	10	01	BRXL		PC ← PC + X[15:0] + 1. X[15:0] sign extended.	-
-	H'0	00	10	ST UX	@(<nn>,y)	@(<nn>,y) ← UX[15:0]	-
-	H'0	01	10	LD UX	@(<nn>,y)	UX[15:0] ← @(<nn>,y)	-
-	H'0	10	10	ST XH	@(<nn>,y)	@(<nn>,y) ← (U==1) ? UX[23:16] : {IX[23:16], UX[23:16]}	-
-	H'0	11	10	LD XH	@(<nn>,y)	(U==1) ? UX[23:16] : {IX[23:16], UX[23:16]} ← @(<nn>,y)	-
-	H'0	00	11	ST UY	@(<nn>,y)	@(<nn>,y) ← UY[15:0]	-
-	H'0	01	11	LD UY	@(<nn>,y)	UY[15:0] ← @(<nn>,y)	-
-	H'1	-	-	LD	reg, data	reg ← data	NZ
-	H'1	-	-	LD.B <sup>†</sup>	reg, data	reg[15:0] ← data[7:0] or data[15:8] sign extended	NZ
-	H'1	-	-	LD.BU <sup>†</sup>	reg, data	reg[15:0] ← data[7:0] or data[15:8] zero extended	NZ
-	H'2	-	00	PRINT	reg, data	None. Debug request for simulators.	-
-	H'2	-	not-00	ST	reg, data	data ← reg	NZ
-	H'2	-	not-00	ST.B <sup>†</sup>	reg, data	data[7:0] ← reg[7:0]	NZ
				MOV	regd,AL	regd[15:0] ← AL[15:0]; regd == X, XH and Y	
				MOV	regx,AH	regx[15:0] ← AH[15:0]; regx == X, and XH	
				MOV	rega, Y	rega[15:0] ← Y[15:0]; rega == AH and AL	
				MOV24	X:,A	XH[7:0] ← AH[7:0], X[15:0] ← AL[15:0]	

**Reg Register Access Field**

<i>Reg field</i>	<i>reg</i>	<i>regd</i>	<i>regx</i>	<i>rega</i>
00	AH			AH
01	AL	XH	XH	AL
10	X	X	X	
11	Y	Y		

† Indicates UNSIGNED prefix instruction required for this instruction.

<nn> represents the instruction operand for instructions with a specific addressing mode.

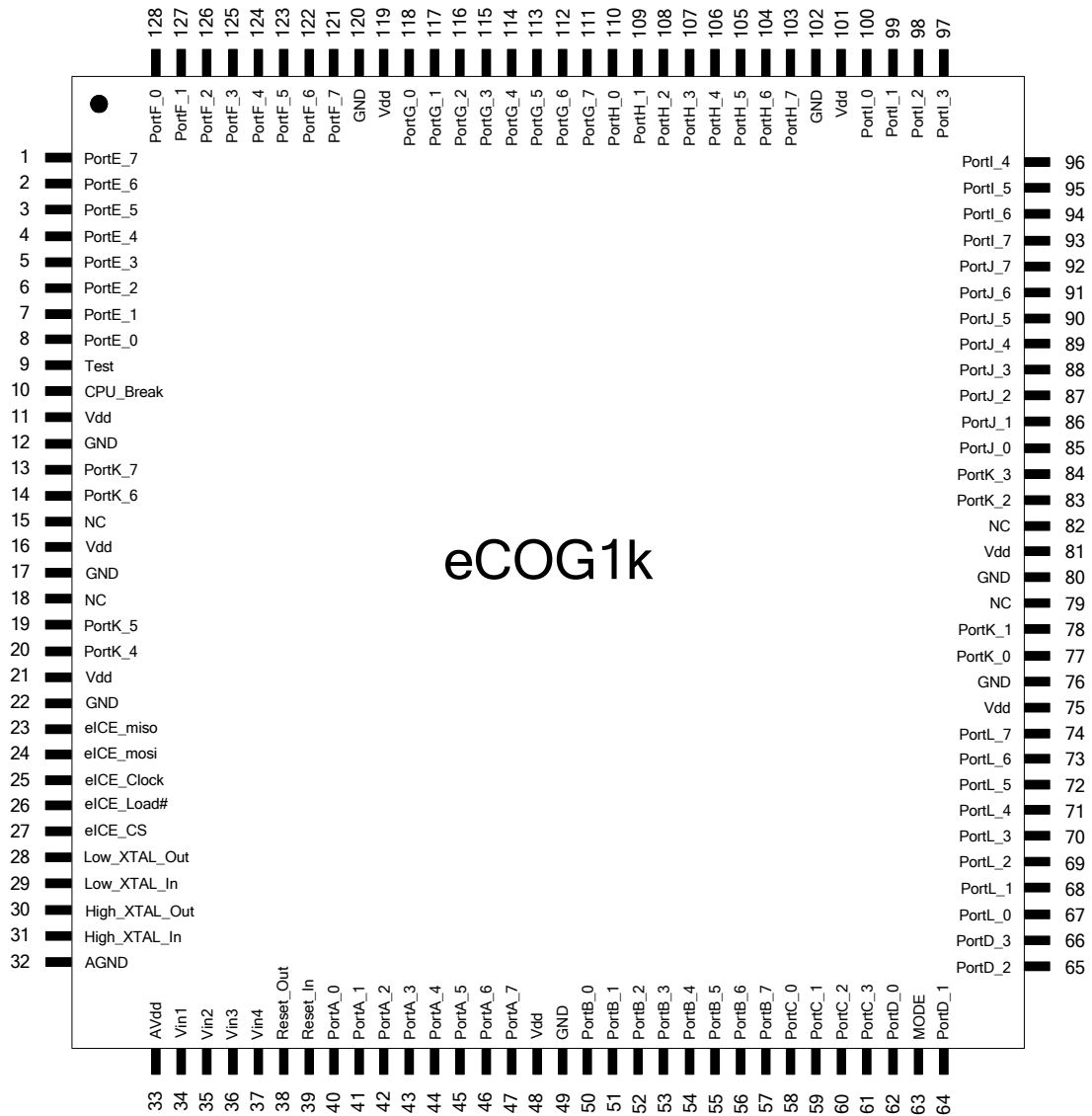
<i>Operand</i>	<i>Opcod</i>	<i>Reg</i>	<i>Mode</i>	<i>Assembler</i>		<i>Operation</i>	<i>Flags</i>
-	H'3	-	-	ADD	reg, data	reg ← reg + data	CSNZ
-	H'4	-	-	ADDC	reg, data	reg ← reg + data + C	CSNZ
-	H'5	-	-	SUB	reg, data	reg ← reg – data	CSNZ
-	H'6	-	-	SUBC	reg, data	reg ← reg – data – C	CSNZ
-	H'7	-	-	NADD	reg, data	reg ← -reg + data	CSNZ
-	H'8	-	-	CMP	reg, data	flags ← reg – data	CSNZ
-	H'9	00	-	UMULT†	data	A ← AL * data	-
-	H'9	00	-	SMULT	data	Sign Extend. A ← AL * data	-
-	H'9	01	-	UDIV†	data	AL ← A ÷ data; AH ← rem	-
-	H'9	01	-	SDIV	data	Sign Extend. AL ← A ÷ data; AH ← rem	-
-	H'9	10	-	TST	data	flags ← data	NZ
-	H'9	11	-	BSR	addr	X ← PC + 1; PC ← branch_addr	-
-	H'A	00	-	ASL	data	C ← [AH, AL] ← 0	C
-	H'A	00	-	LSL	data	C ← [AH, AL] ← 0	C
-	H'A	01	-	ASR	data	AH[15] → [AH, AL] → C	C
-	H'A	01	-	LSR†	data	0 → [AH, AL] → C	C
-	H'A	10	-	ROL	data	C ← [AH, AL] ← C	C
-	H'A	11	-	ROR	data	C → [AH, AL] → C	C
-	H'B	-	-	OR	reg, data	reg ← reg   data	NZ
-	H'C	-	-	AND	reg, data	reg ← reg & data	NZ
-	H'D	-	-	XOR	reg, data	reg ← reg ^ data	NZ
-	H'E	00	-	BRA	addr	PC ← branch_addr	-
-	H'E	01	-	BLT	addr	if S = 1 PC ← branch_addr	-
-	H'E	10	-	BPL	addr	if N = 0 PC ← branch_addr	-
-	H'E	11	-	BMI	addr	if N = 1 PC ← branch_addr	-
-	H'F	00	-	BNE	addr	if Z = 0 PC ← branch_addr	-
-	H'F	01	-	BEQ	addr	if Z = 1 PC ← branch_addr	-
-	H'F	10	-	BCC	addr	if C = 0 PC ← branch_addr	-
-	H'F	11	-	BCS	addr	if C = 1 PC ← branch_addr	-

**Mode Field**

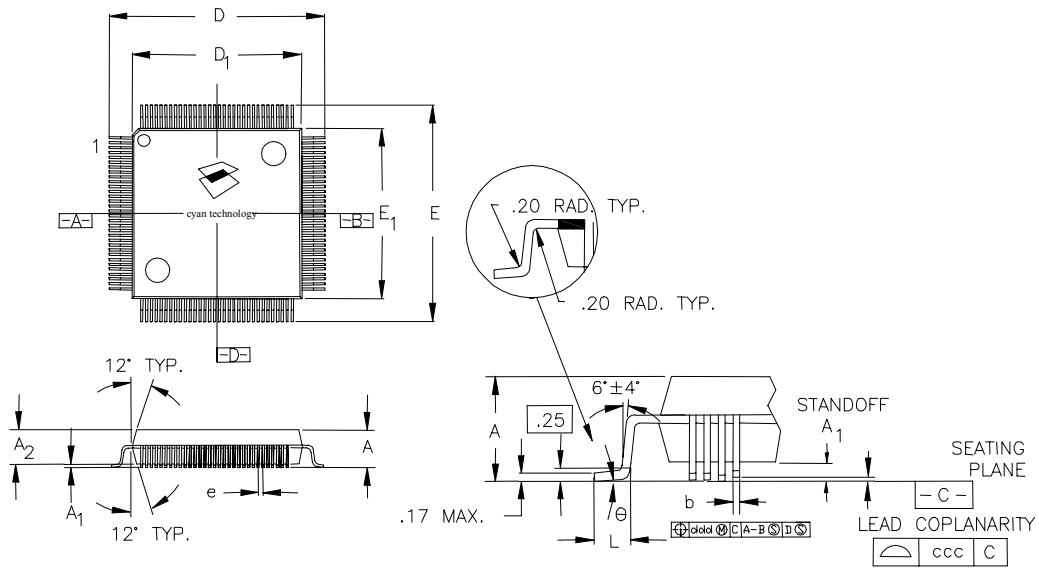
<i>mode</i>	<b>Data Mode: Source or Destination</b>	
00	Immediate	data = 16-bit sign extended operand
01	Direct	data = 16-bit value @ 16-bit operand address
10	Indexed X	data = 16-bit value @ X+16-bit operand address
11	Indexed Y	data = 16-bit value @ Y+16-bit operand address
<i>mode</i>	<b>Data Mode Byte Accesses: Source or Destination</b>	
00	unused	
01	Direct	data = 8-bit value @ 17-bit operand byte address
10	Indexed X	data = 8-bit value @ 17-bit byte address in {XH,X}+17-bit operand byte address
11	Indexed Y	data = 8-bit value @ 16-bit word address in Y+17-bit operand byte address
<i>mode</i>	<b>Address Mode: Branch Address</b>	
00	PC relative	PC + 24-bit operand
01	Direct	{XH, @ 16-bit operand address}
10	X Relative	{XH, X} + 24-bit sign extended operand
11	Indexed Y	{XH, @(Y + 16-bit operand)}

### Pinout of eCOG1k

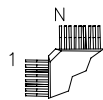
128 pin LQFP. Pin pitch 0.4mm. 14x14mm body. 16x16mm at pin edge.



Package Drawing



ANOTHER VARIATION OF PIN 1 VISUAL AID



- NOTES: 1) ALL DIMENSIONS IN MM.  
 2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED.  
 3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") OR 0.15 MM (.006") THICK.  
 4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

BODY + 2.00 mm FOOTPRINT		
DIMS.	LEADS	
	TOL.	L/F
A	MAX.	1.60
A <sub>1</sub>	.05 MIN./ .15 MAX.	
A <sub>2</sub>	±.05	1.40
D	±.20	16.00
D <sub>1</sub>	±.05	14.00
E	±.20	16.00
E <sub>1</sub>	±.05	14.00
L	+ .15 / - .10	.60
e	BASIC	.40
b	±.05	.18
θ	0° - 7°	
ddd	MAX.	.07
ccc	MAX.	.08

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I<sup>2</sup>C, I<sup>2</sup>C and the I<sup>2</sup>C interface are patented by Philips Semiconductor in certain territories. Philips may demand a royalty or licence fee from designs using the I<sup>2</sup>C interface.

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