

Preliminary Technical Data

ADG821/ADG822/ADG823

FEATURES

- Low On Resistance <math><0.8 \Omega</math> max at 5 V supply
- 0.2 Ω max On-Resistance Flatness
- +1.8 V to +5.5 V Single Supply
- Extended Temperature Range: +125°C
- High Current Carrying Capability
- Rail-to-Rail Operation
- 8-Lead μ SOIC Package
- Fast Switching Times
- Typical Power Consumption (<math><0.01 \mu\text{W}</math>)
- TTL/CMOS Compatible Inputs
- Pin Compatible with ADG721/722/723

APPLICATIONS

- Power Routing
- Battery Powered Systems
- Communication Systems
- Data Acquisition Systems
- Audio and Video Signal Routing
- Cellular Phones
- Modems
- PCMCIA Cards
- Hard Drives
- Audio and Video Switching
- Relay Replacement

GENERAL DESCRIPTION

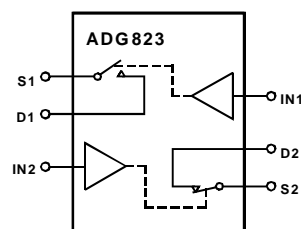
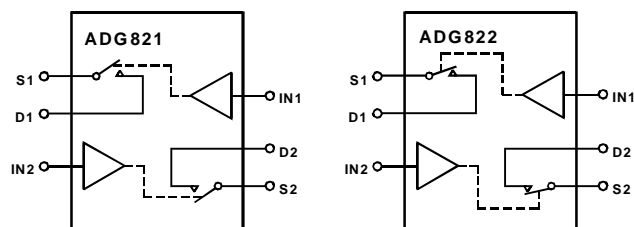
The ADG821, ADG822 and ADG823 are monolithic CMOS SPST (single pole, single throw) switches. These switches are designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low On Resistance and low leakage currents.

The ADG821, ADG822 and ADG823 are designed to operate from a single +1.8 V to +5.5 V supply, making them ideal for use in battery powered instruments.

Each switch of the ADG821/2/3 conducts equally well in both directions when on. The ADG821, ADG822 and ADG823 contain two independent SPST switches. The ADG821 and ADG822 differ only in that both switches are normally open and normally closed respectively. In the ADG823, Switch 1 is normally open and Switch 2 is normally closed. The ADG823 exhibits break-before-make switching action.

The ADG821, ADG822 and ADG823 are available in an 8-lead μ SOIC package.

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "0" INPUT

PRODUCT HIGHLIGHTS

1. Very Low On Resistance (0.5 Ω typical).
2. On-Resistance Flatness ($R_{\text{FLAT(ON)}}$) (0.1 Ω typ).
3. Low Power Dissipation. CMOS construction ensures low power dissipation.
4. High Current Carrying Capability.
5. 8-Lead μ SOIC Package.

REV. PrF 01/02

ADG821/822/823 – SPECIFICATIONS¹ (V_{DD} = +5 V ± 10%, GND = 0 V. All specifications –40°C to +125°C, unless otherwise noted.)

| Parameter | +25°C | –40°C to +85°C | –40°C to +125°C | Units | Test Conditions/Comments |
|---|---------------|----------------|------------------------|------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V _{DD} | V | |
| On Resistance (R _{ON}) | 0.5 0.8 | 1 | 1.5 | Ω typ Ω max | V _S = 0 V to V _{DD} , I _S = –10 mA, Test Circuit 1 |
| On Resistance Match Between Channels (ΔR _{ON}) | 0.06 0.12 | 0.1 0.15 | | Ω typ Ω max | V _S = 0 V to V _{DD} , I _S = –10 mA |
| On-Resistance Flatness (R _{FLAT(ON)}) | 0.1 | 0.2 | 0.3 | Ω typ Ω max | V _S = 0 V to V _{DD} , I _S = –10 mA |
| LEAKAGE CURRENTS | | | | | |
| Source OFF Leakage I _S (OFF) | ±0.01 ±0.5 | ±1 | TBD | nA typ nA max | V _{DD} = +5.5 V V _S = 4.5 V/1 V, V _D = 1 V/4.5 V Test Circuit 2 |
| Drain OFF Leakage I _D (OFF) | ±0.01 ±0.5 | ±1 | TBD | nA typ nA max | V _S = 4.5 V/1 V, V _D = 1 V/4.5 V Test Circuit 2 |
| Channel ON Leakage I _D , I _S (ON) | ±0.01 ±0.5 | ±1 | TBD | nA typ nA max | V _S = V _D = 1 V, or V _S = V _D = 4.5 V Test Circuit 3 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V _{INH} | | | 2.4 | V min | |
| Input Low Voltage, V _{INL} | | | 0.8 | V max | |
| Input Current I _{INL} or I _{INH} | 0.005 | | ±0.1 | μA typ μA max | V _{IN} = V _{INL} or V _{INH} |
| DYNAMIC CHARACTERISTICS² | | | | | |
| t _{ON} | 30 TBD | | TBD | ns typ ns max | R _L = 50 Ω, C _L = 35 pF V _S = 3 V, Test Circuit 4 |
| t _{OFF} | 20 TBD | | TBD | ns typ ns max | R _L = 50 Ω, C _L = 35 pF V _S = 3 V, Test Circuit 4 |
| Break-Before-Make Time Delay, t _{BBM} (ADG823 Only) | 10 | | TBD | ns typ ns min | R _L = 50 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 3 V, Test Circuit 5 |
| Charge Injection | ±20 | | | pC typ | V _S = 0 V; R _S = 0 Ω, C _L = 1 nF, Test Circuit 6 |
| Off Isolation | –65 | | | dB typ | R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, Test Circuit 7 |
| Channel-to-Channel Crosstalk | –65 | | | dB typ | R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, Test Circuit 9 |
| Bandwidth –3 dB | 30 | | | MHz typ | R _L = 50 Ω, C _L = 5 pF, Test Circuit 8 |
| C _S (OFF) | 25 | | | pF typ | |
| C _D (OFF) | 25 | | | pF typ | |
| C _D , C _S (ON) | 75 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| I _{DD} | 0.001 | | 1.0 | μA typ μA max | V _{DD} = +5.5 V Digital Inputs = 0 V or 5.5 V |

NOTES

¹Temperature ranges are as follows: Extended Range: –40°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG821/822/823 –SPECIFICATIONS¹

(V_{DD} = +2.7 V to +3.6 V, GND = 0 V. All specifications –40°C to +125°C, unless otherwise noted.)

| Parameter | +25°C | –40°C to +85°C | –40°C to +125°C | Units | Test Conditions/Comments |
|---|-------|-------------------|------------------------|------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V _{DD} | V | V _S = 0 V to V _{DD} , I _S = –10 mA Test Circuit 1 |
| On Resistance (R _{ON}) | 1 | | | Ω typ | |
| | 1.6 | 2 | 2.5 | Ω max | |
| On Resistance Match Between Channels (ΔR _{ON}) | 0.1 | | | Ω typ | V _S = 0 V to V _{DD} , I _S = –10 mA |
| On-Resistance Flatness (R _{FLAT(ON)}) | 0.2 | | TBD | Ω typ | V _S = 0 V to V _{DD} , I _S = –10 mA |
| LEAKAGE CURRENTS | | | | | |
| Source OFF Leakage I _S (OFF) | ±0.01 | | | nA typ | V _{DD} = +3.3 V |
| | ±0.5 | ±1 | TBD | nA max | V _S = 3 V/1 V, V _D = 1 V/3 V |
| Drain OFF Leakage I _D (OFF) | ±0.01 | | | nA typ | V _S = 3 V/1 V, V _D = 1 V/3 V |
| | ±0.5 | ±1 | TBD | nA max | Test Circuit 2 |
| Channel ON Leakage I _D , I _S (ON) | ±0.01 | | | nA typ | V _S = V _D = 1 V, or 3 V |
| | ±0.5 | ±1 | TBD | nA max | Test Circuit 3 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V _{INH} | | | 2.0 | V min | V _{IN} = V _{INL} or V _{INH} |
| Input Low Voltage, V _{INL} | | | 0.4 | V max | |
| Input Current | | | | | |
| I _{INL} or I _{INH} | 0.005 | | ±0.1 | μA typ μA max | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| t _{ON} | 50 | | | ns typ | R _L = 50 Ω, C _L = 35 pF |
| | TBD | | TBD | ns max | V _S = 1.5 V, Test Circuit 4 |
| t _{OFF} | 40 | | | ns typ | R _L = 50 Ω, C _L = 35 pF |
| | TBD | | TBD | ns max | V _S = 1.5 V, Test Circuit 4 |
| Break-Before-Make Time Delay, t _{BBM} (ADG823 Only) | 10 | | | ns typ | R _L = 50 Ω, C _L = 35 pF, |
| | | | TBD | ns min | V _{S1} = V _{S2} = 2 V, Test Circuit 5 |
| Charge Injection | ±20 | | | pC typ | V _S = 0 V; R _S = 0 Ω, C _L = 1 nF, Test Circuit 6 |
| Off Isolation | –65 | | | dB typ | R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, Test Circuit 7 |
| Channel-to-Channel Crosstalk | –65 | | | dB typ | R _L = 50 Ω, C _L = 5 pF, f = 1 MHz, Test Circuit 9 |
| Bandwidth –3 dB | 30 | | | MHz typ | R _L = 50 Ω, C _L = 5 pF, Test Circuit 8 |
| C _S (OFF) | 25 | | | pF typ | |
| C _D (OFF) | 25 | | | pF typ | |
| C _D , C _S (ON) | 75 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| I _{DD} | 0.001 | | 1.0 | μA typ μA max | V _{DD} = +3.3 V Digital Inputs = 0 V or 3.3 V |

NOTES

¹Temperature ranges are as follows: Extended Range: –40°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG821/ADG822/ADG823

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

| | |
|--|--|
| V _{DD} to V _{SS} | 7 V |
| V _{DD} to GND | -0.3 V to +7 V |
| V _{SS} to GND | +0.3 V to -3.5 V |
| Analog Inputs ² | V _{SS} - 0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First |
| Digital Inputs ² | -0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First |
| Peak Current, S or D | 400 mA (Pulsed at 1 ms, 10% Duty Cycle max) |
| Continuous Current, S or D | 200 mA |
| Operating Temperature Range | |
| Extended | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | +150°C |

8-Lead μSOIC Package

| | |
|--|---------|
| θ _{JA} Thermal Impedance | 206°C/W |
| θ _{JC} Thermal Impedance | 44°C/W |
| Lead Temperature, Soldering (10 seconds) | 300°C |
| IR Reflow, Peak Temperature | +220°C |

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table 1. Truth Table for the ADG821/22

| ADG821 IN _x | ADG822 IN _x | Switch x Condition |
|------------------------|------------------------|--------------------|
| 0 | 1 | OFF |
| 1 | 0 | ON |

Table 2. Truth Table for the ADG823

| IN1 | IN2 | Switch S1 | Switch S2 |
|-----|-----|-----------|-----------|
| 0 | 0 | OFF | ON |
| 0 | 1 | OFF | OFF |
| 1 | 0 | ON | ON |
| 1 | 1 | ON | OFF |

ORDERING GUIDE

| Model Option | Temperature Range | Supply Option | Brand ¹ | Package Description | Package |
|--------------|-------------------|---------------|--------------------|-------------------------------|---------|
| ADG821BRM | -40°C to +125°C | 3 V, 5 V | SQB | μSOIC (microSmall Outline IC) | RM-8 |
| ADG822BRM | -40°C to +125°C | 3 V, 5 V | SRB | μSOIC (microSmall Outline IC) | RM-8 |
| ADG823BRM | -40°C to +125°C | 3 V, 5 V | SSB | μSOIC (microSmall Outline IC) | RM-8 |

¹Branding on μSOIC packages is limited to three characters due to space constraints.

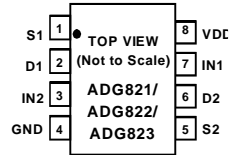
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG821/822/823 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION

8-Lead μ SOIC
(RM-8)

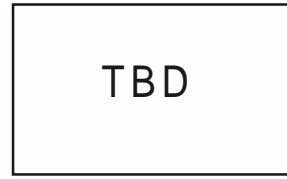


TERMINOLOGY

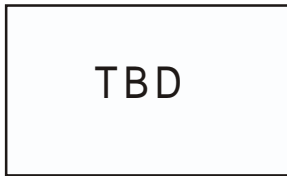
| | |
|--------------------|--|
| V_{DD} | Most Positive Power Supply Potential. |
| V_{SS} | Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device. |
| GND | Ground (0 V) Reference. |
| I_{DD} | Positive Supply Current. |
| I_{SS} | Negative Supply Current. |
| S | Source Terminal. May be an input or output. |
| D | Drain Terminal. May be an input or output. |
| IN | Logic Control Input. |
| R_{ON} | Ohmic resistance between D and S. |
| ΔR_{ON} | On resistance match between any two Channels i.e., $R_{ON\ max} - R_{ON\ min}$. |
| $R_{FLAT(ON)}$ | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| I_S (OFF) | Source Leakage Current with the switch "OFF." |
| I_D (OFF) | Drain Leakage Current with the switch "OFF". |
| I_D, I_S (ON) | Channel Leakage Current with the switch "ON." |
| $V_D (V_S)$ | Analog Voltage on Terminals D, S. |
| V_{INL} | Maximum Input Voltage for Logic "0". |
| V_{INH} | Minimum Input Voltage for Logic "1". |
| $I_{INL}(I_{INH})$ | Input Current of the digital Input. |
| C_S (OFF) | "OFF" Switch Source Capacitance. |
| C_D (OFF) | "OFF" Switch Drain Capacitance. |
| C_D, C_S (ON) | "ON" Switch Capacitance. |
| t_{ON} | Delay between applying the digital control input and the output switching on. |
| t_{OFF} | Delay between applying the digital control input and the output switching off. |
| t_{BBM} | "OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. |
| Charge Injection | A measure of the Glitch Impulse transferred from the Digital input to the Analog output during switching. |
| Crosstalk | A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. |
| Off Isolation | A measure of unwanted signal coupling through an "OFF" switch. |
| Bandwidth | The frequency at which the output is attenuated by -3 dBs. |
| On Response | The frequency response of the "ON" switch. |
| Insertion Loss | The Loss due to the ON resistance of the Switch. |



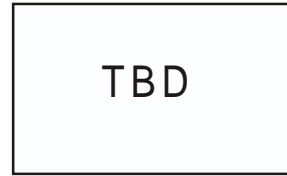
TPC 1.



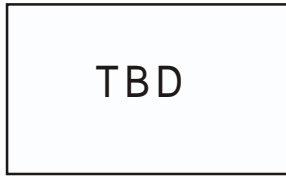
TPC 2.



TPC 3.



TPC 4.



TPC 5.

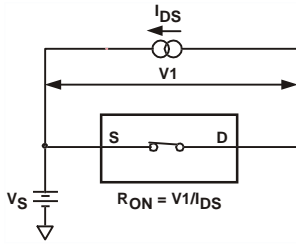


TPC 6.

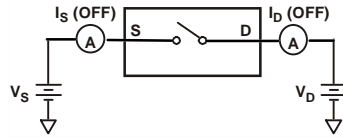


TPC 7.

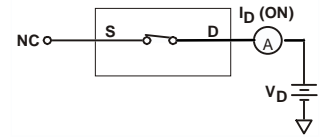
Test Circuits



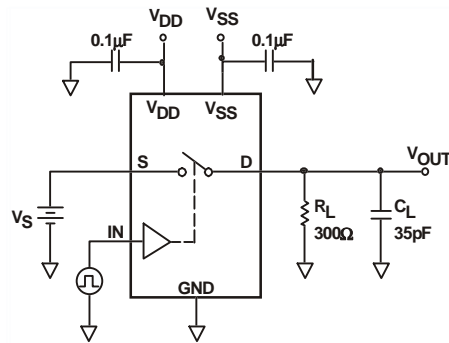
Test Circuit 1. On Resistance



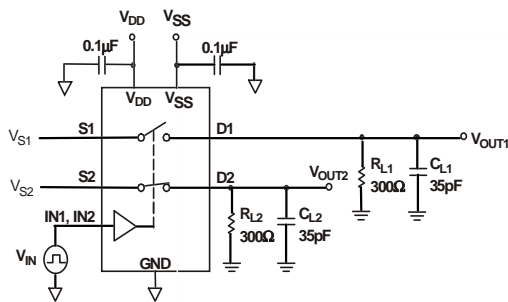
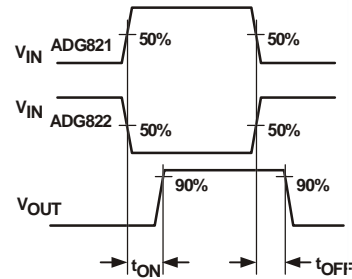
Test Circuit 2. Off Leakage



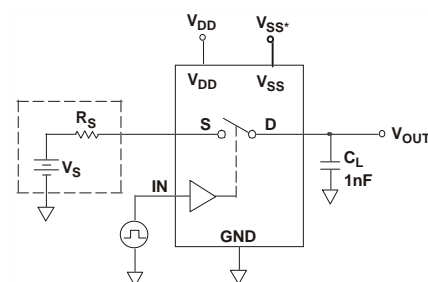
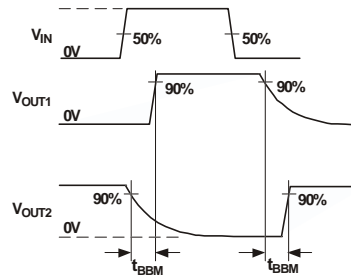
Test Circuit 3. On Leakage



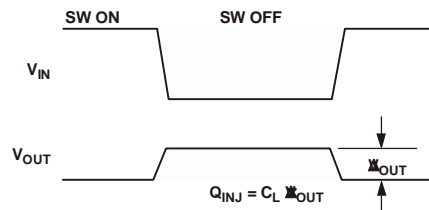
Test Circuit 4. Switching Times



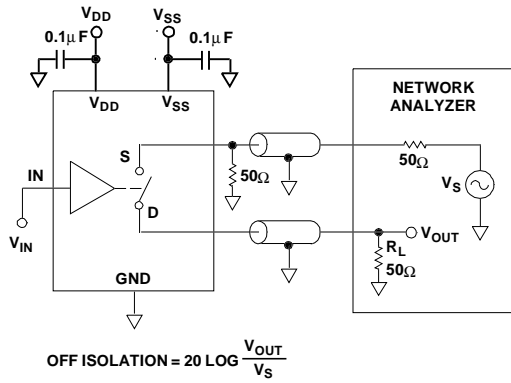
Test Circuit 5. Break-Before-Make time Delay, t_{BBM} (ADG823 only)



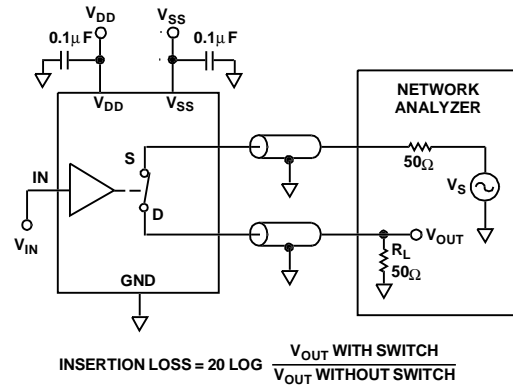
Test Circuit 6. Charge Injection



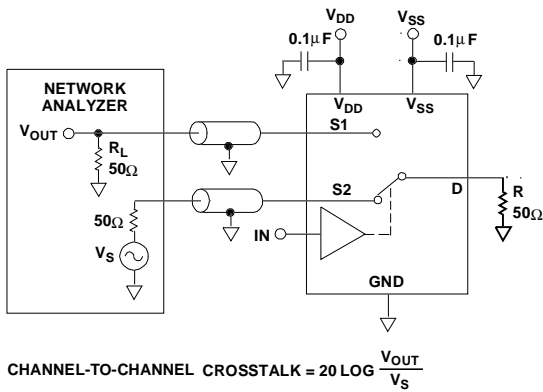
ADG821/ADG822/ADG823



Test Circuit 7. Off Isolation



Test Circuit 8. Bandwidth



Test Circuit 9. Channel-to-Channel Crosstalk

ADG821/ADG822/ADG823

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead μ SOIC (RM-8)

