

Preliminary Technical Data**ADG819/820****FEATURES**

Low On Resistance <0.8 Ω max at 5 V supply
0.2 Ω max On-Resistance Flatness
+1.8 V to +5.5 V Single Supply
High Current Carrying Capability
Extended Temperature Range: +125°
Rail-to-Rail Operation
6-Lead SOT-23 Package, 8-Lead μ SOIC Package,
Wafer-Level Chipscale Package
Fast Switching Times
Typical Power Consumption (<0.01 μ W)
TTL/CMOS Compatible Inputs
Pin Compatible with the ADG719 (ADG819)

APPLICATIONS

Power Routing
Battery Powered Systems
Communication Systems
Data Acquisition Systems
Audio and Video Signal Routing
Cellular Phones
Modems
PCMCIA Cards
Hard Drives
Audio and Video Switching
Relay Replacement

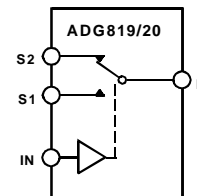
GENERAL DESCRIPTION

The ADG819 and the ADG820 are monolithic, CMOS SPDT (single pole, double throw) switches. These switches are designed on a submicron process, that provides low power dissipation yet gives high switching speed, low On Resistance and low leakage currents.

Low-power consumption and operating supply range of +1.8 V to +5.5 V make the ADG819 and ADG820 ideal for battery-powered, portable instruments.

Each switch of the ADG819/820 conducts equally well in both directions when on. The ADG819 exhibits break-before-make switching action, thus preventing momentary shorting when switching channels. The ADG820 exhibits make-before-break action.

The ADG819/820 are available in a 6-lead SOT-23 package and an 8-lead μ SOIC package. The ADG819 is also available in a 2x3 array Wafer-level Chipscale package. This chip occupies only a 2.18mm x 1.14mm area, thus making it the ideal candidate for space-constrained applications.

FUNCTIONAL BLOCK DIAGRAM

SWITCHES SHOWN FOR A LOGIC "1" INPUT

PRODUCT HIGHLIGHTS

1. Very Low On Resistance, 0.5 Ω typical.
2. +1.8 V to +5.5 V Single Supply Operation.
3. Low Power Dissipation. CMOS construction ensures low power dissipation.
4. High Current Carrying Capability.
5. Tiny 6-Lead SOT-23 Package, 8-Lead μ SOIC Package and 2x3 array Wafer-level Chipscale Package.

REV. PrF 01/02

ADG819/820—SPECIFICATIONS¹

($V_{DD} = +5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+125^\circ\text{C}$ unless otherwise noted.)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.5 0.8		1	Ω typ Ω max	$V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$ Test Circuit 1
On Resistance Match Between Channels (ΔR_{ON})	0.06 0.12	0.1 0.15	0.2	Ω typ Ω max	$V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.1	0.2	0.25	Ω typ Ω max	$V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.5	± 1	TBD	nA typ nA max	$V_{DD} = +5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$ Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01 ± 0.5	± 1	TBD	nA typ nA max	$V_S = V_D = 1\text{ V}$, or $V_S = V_D = 4.5\text{ V}$ Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
DYNAMIC CHARACTERISTICS²					
t_{ON}	30 TBD		TBD	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 4
t_{OFF}	20 TBD		TBD	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 4
ADG819					
Break-Before-Make Time Delay, t_{BBM}	10		TBD	ns typ ns min	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$, Test Circuit 5
ADG820					
Make-Before-Break Time Delay, t_{MBS}	15		TBD	ns typ ns min	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 0\text{ V}$, Test Circuit 6
Charge Injection	± 20			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ Test Circuit 7
Off Isolation	-65			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 8
Channel-to-Channel Crosstalk	-65			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 10
Bandwidth -3 dB	30			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	25			pF typ	
C_D , C_S (ON)	75			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	μA typ μA max	$V_{DD} = +5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V

NOTES

¹Temperature ranges are as follows: Extended Range: -40°C to $+125^\circ\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG819/820–SPECIFICATIONS¹ ($V_{DD} = +2.7\text{ V to }+3.6\text{ V}$, $GND = 0\text{ V}$. All specifications $-40^{\circ}\text{C to }+125^{\circ}\text{C}$ unless otherwise noted.)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	$V_S = 0\text{ V to }V_{DD}$, $I_S = -10\text{ mA}$, Test Circuit 1
On Resistance (R_{ON})	1 1.6		2	Ω typ Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	$V_S = 0\text{ V to }V_{DD}$, $I_S = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.2		TBD	Ω typ	$V_S = 0\text{ V to }V_{DD}$, $I_S = -10\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.01 ± 0.5	± 1	TBD	nA typ nA max	$V_{DD} = +3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$, Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.01 ± 0.5	± 1	TBD	nA typ nA max	$V_S = V_D = 1\text{ V}$, or $V_S = V_D = 3\text{ V}$, Test Circuit 3
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}			0.4	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	
DYNAMIC CHARACTERISTICS²					
t_{ON}	50 TBD		TBD	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$, Test Circuit 4
t_{OFF}	40 TBD		TBD	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$, Test Circuit 4
ADG819 Break-Before-Make Time Delay, t_{BBM}	10		TBD	ns typ ns min	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 1.5\text{ V}$, Test Circuit 5
ADG820 Make-Before-Break Time Delay, t_{MBB}	15		TBD	ns typ ns min	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 1.5\text{ V}$, Test Circuit 6
Charge Injection	± 20			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, Test Circuit 7
Off Isolation	-65			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 8
Channel-to-Channel Crosstalk	-65			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, Test Circuit 10
Bandwidth -3 dB	30			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	25			pF typ	
C_D , C_S (ON)	75			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	μA typ μA max	$V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V

NOTES

¹Temperature ranges are as follows: Extended Range: $-40^{\circ}\text{C to }+125^{\circ}\text{C}$.

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ADG819/820

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to GND	-0.3 V to +7 V
Analog Inputs ²	-0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs ²	-0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	400 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	200 mA
Operating Temperature Range	
Extended	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
μSOIC Package	
θ _{JA} Thermal Impedance	206°C/W
θ _{JC} Thermal Impedance	44°C/W
SOT-23 Package	
θ _{JA} Thermal Impedance	229.6°C/W
θ _{JC} Thermal Impedance	91.99°C/W

WLCSP Package

θ _{JA} Thermal Impedance	°C/W
θ _{JC} Thermal Impedance	°C/W
Lead Temperature, Soldering (10 seconds)	300°C
IR Reflow, Peak Temperature	+220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table for the ADG819/ADG820

IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

ORDERING GUIDE

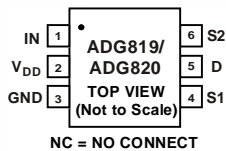
Model Option	Temperature Range	Supply Option	Brand ¹	Package Description	Package
ADG819BRM	-40°C to +125°C	3 V, 5 V	SNB	μSOIC (microSmall Outline IC)	RM-8
ADG819BRT	-40°C to +125°C	3 V, 5 V	SNB	SOT-23 (Plastic Surface Mount)	RT-6
ADG819BCB	-40°C to +85°C	3 V, 5 V	SNB	WLCSP (Wafer-Level Chip Scale Package)	CB-6*
ADG820BRM	-40°C to +125°C	3 V, 5 V	SPB	μSOIC (microSmall Outline IC)	RM-8
ADG820BRT	-40°C to +125°C	3 V, 5 V	SPB	SOT-23 (Plastic Surface Mount)	RT-6

¹Branding on all packages is limited to three characters due to space constraints.

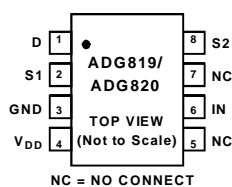
*Contact factory for availability

PIN CONFIGURATIONS

6-Lead SOT-23 (RT-6)

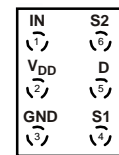


8-Lead μSOIC (RM-8)



2x3 WLCSP

TOP VIEW (bumps at the bottom). Not to Scale



ADG819 Only

TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
I_{DD}	Positive Supply Current.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two Channels i.e., $R_{ON\ max} - R_{ON\ min}$.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the switch "OFF."
I_D, I_S (ON)	Channel Leakage Current with the switch "ON."
V_D (V_S)	Analog Voltage on Terminals D, S.
V_{INL}	Maximum Input Voltage for Logic "0".
V_{INH}	Minimum Input Voltage for Logic "1".
I_{INL} (I_{INH})	Input Current of the digital Input.
C_S (OFF)	"OFF" Switch Source Capacitance.
C_D, C_S (ON)	"ON" Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_{BBM}	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
t_{MBB}	"ON" time, measured between the 80% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the Glitch Impulse transferred from the Digital input to the Analog output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Bandwidth	The frequency at which the output is attenuated by -3 dBs.
On Response	The frequency response of the "ON" switch.
Insertion Loss	The Loss due to the ON resistance of the Switch.

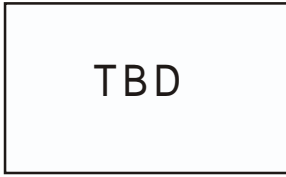
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG819/820 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADG819/820

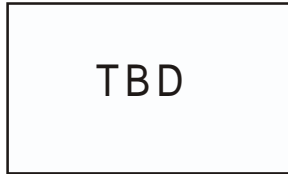
Typical Performance Characteristics



TPC 1.



TPC 2.



TPC 3.



TPC 4.



TPC 5.

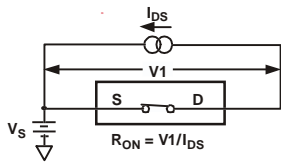


TPC 6.

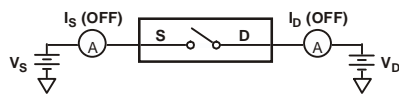


TPC 7.

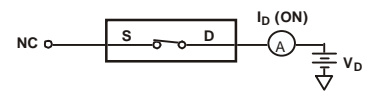
Test Circuits



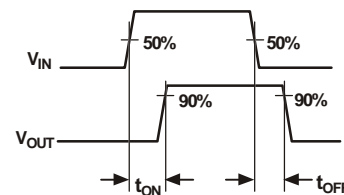
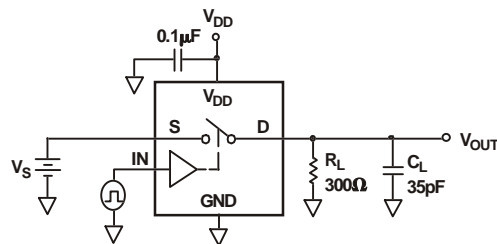
Test Circuit 1. On Resistance



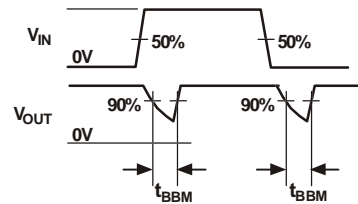
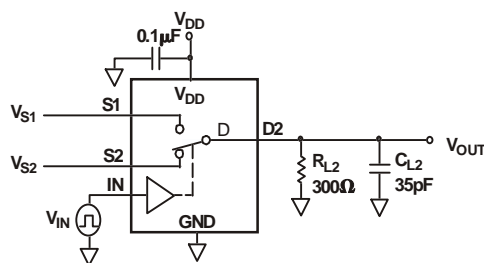
Test Circuit 2. Off Leakage



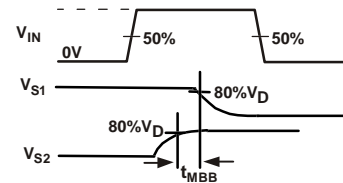
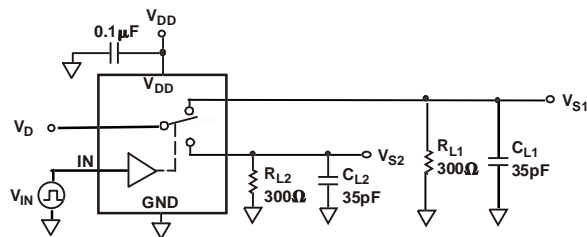
Test Circuit 3. On Leakage



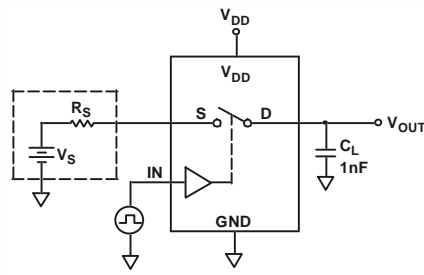
Test Circuit 4. Switching Times



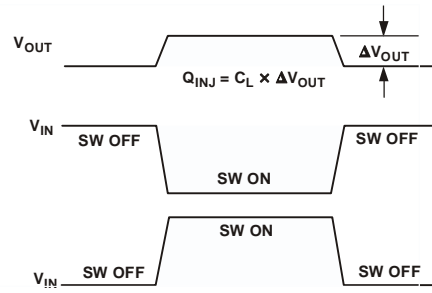
Test Circuit 5. Break-Before-Make Time Delay, t_{BBM} (ADG819 only)



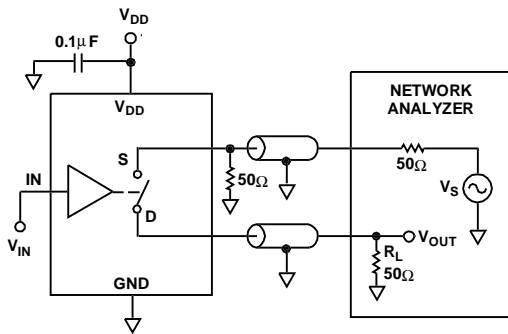
Test Circuit 6. Make-Before-Break Time Delay, t_{MBB} (ADG820 only)



$$\text{CHARGE INJECTION} = \Delta V_{\text{OUT}} \times C_L$$

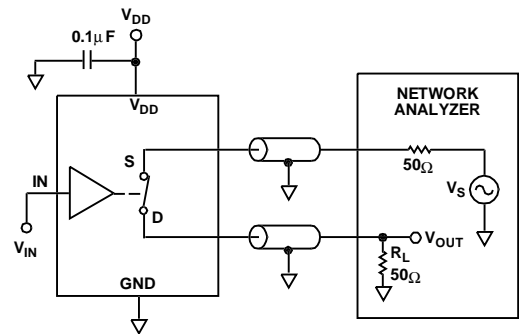


Test Circuit 7. Charge Injection



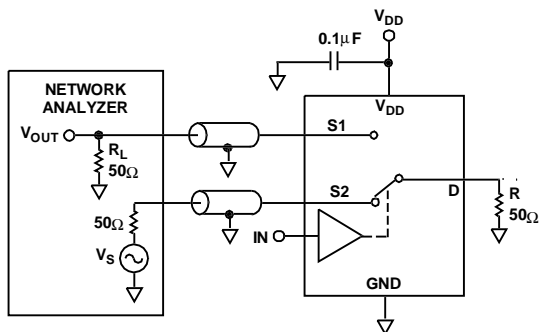
$$\text{OFF ISOLATION} = 20 \text{ LOG} \frac{V_{\text{OUT}}}{V_s}$$

Test Circuit 8. Off Isolation



$$\text{INSERTION LOSS} = 20 \text{ LOG} \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Test Circuit 9. Bandwidth



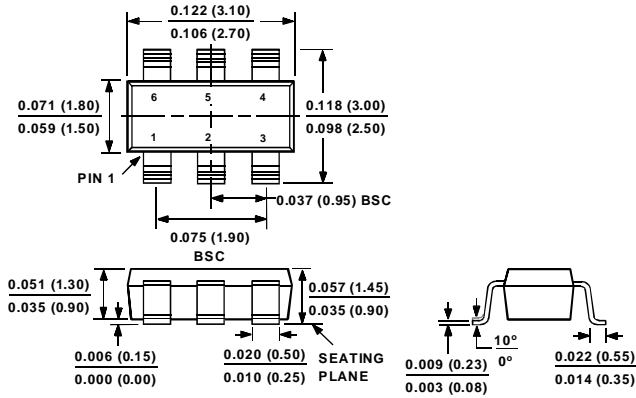
$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \text{ LOG} \frac{V_{\text{OUT}}}{V_s}$$

Test Circuit 10. Channel-to-Channel Crosstalk

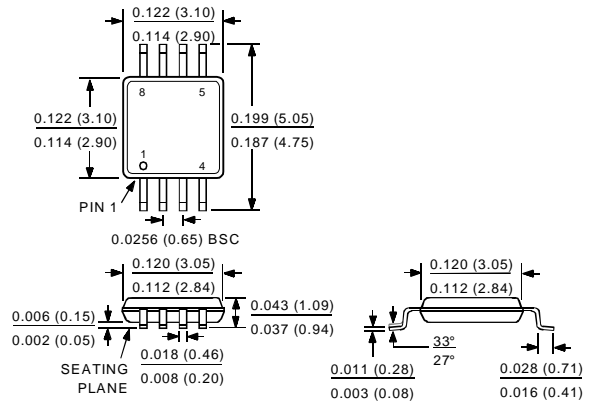
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead Plastic Surface Mount Package (RT-6)



8-Lead μ SOIC Package (RM-8)



2x3 Array for WLCSP (CB-6)

