



16-Bit Sigma-Delta ADC with Programmable Post Processor

Preliminary Technical Data

AD7725

FEATURES

Programmable Filtering:
Any characteristic up to 108 tap FIR and/or IIR
Polynomial Signal Conditioning up to 8th Order
Programmable Decimation and Output Word Rate
Flexible Programming Modes
Parallel/Serial Interface
Boot from ROM (BFR) - Internal Default Filter
Boot from DSP or External EPROM
19.2 MHz Max Master Clock Frequency
0 to +4V (Single Ended) or $\pm 2V$ (Differential) Input Range
Power Supplies: AV_{DD} , DV_{DD} : +5V \pm 5%
On-Chip 2.5V Voltage Reference
44-Pin PQFP Package

TYPICAL APPLICATIONS

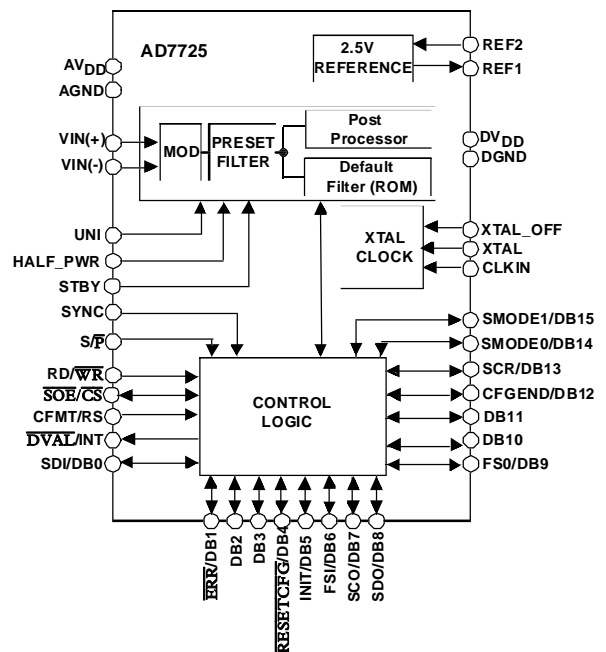
Radar
Sonar
Auxillary Car Functions
Medical Communications

GENERAL DESCRIPTION

The AD7725 is a complete 16-bit, sigma-delta analog to digital converter with on chip user-programmable signal conditioning. The output of the modulator is processed by three cascaded finite impulse response (FIR) filters. This is followed by a user-programmable post processor. The user has complete control over the filter response (lowpass, highpass, bandpass, stopband), the filter coefficients and the decimation ratio. The post processor accepts up to 108 coefficients. The AD7725 provides 16-bit performance for input bandwidths up to 460 kHz and an output word rate of 1.2 MHz maximum. The input sample rate is set either by the crystal oscillator or an external clock. The output is available via a serial or parallel interface.

The device contains a post processor which permits the signal conditioning characteristics to be programmed through the parallel microprocessor interface, through a serial interface or, it may boot at power-on-reset from its default filter (internal ROM) or from an external serial EPROM.

FUNCTIONAL BLOCK DIAGRAM



The post processor is a fully programmable core which provides processing power of up to 130 million accumulates (MAC) per second. To program the post processor, either the on-board default filter or a user defined filter in the form of a configuration file can be loaded. The configuration file can be generated by a digital filter design package called 'Filter Wizard' which is available from Systolix (www.systolix.co.uk). This package allows the user to design different filter types and generates the appropriate configuration file to be downloaded to the postprocessor.

This part provides an accurate on-chip 2.5 V reference for the modulator. A reference input/output function is provided to allow either the internal reference or an external system reference to be used as the reference source for the modulator.

The device is offered in a 44-pin PQFP package and is designed to operate from -40°C to +85°C.

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SPECIFICATIONS¹

($V_{DD} = +5V \pm 5\%$; $AGND = AGND1 = AGND2 = DGND = 0V$;
 $F_{CLKIN} = 19.2 \text{ MHz}$; $REF2 = 2.5 \text{ V}$; $T_A = T_{MIN}$ to T_{MAX} ; unless otherwise noted)

Parameter	Test Conditions/Comments	Min	B Version Typ	Max	Units
DYNAMIC SPECIFICATIONS²					
PRESET FILTER OUTPUT	HALF_PWR = 0 or 1 $f_{CLKIN} = 9.6\text{MHz}$ when HALF_PWR = 1 $F_{IN} = 10\text{kHz}$ See Figure 1				
Noise Analysis	0 to fs/4		-135	-132	dBc/Hz
Noise relative to a Carrier	Serial	79			dB
RMS noise (fs/4 to 3fs/8)	Parallel	84			dB
RMS noise (3fs/8 to fs/2)	Serial	78			dB
RMS noise (3fs/8 to fs/2)	Parallel	79			dB
Total Harmonic Distortion ^{3,4}				-88	dB
Spurious Free Dynamic Range ^{3,4}				-90	dB
DEFAULT FILTER					
Internal ROM FIR Filter					
Bipolar Mode					
Signal to Noise ⁴	Measurement Bandwidth = $0.383 \times F_O$ 2.5V Reference	82	86		dB
Signal to Noise ⁴	3V Reference	83	87		dB
Signal to Noise ⁴	Measurement Bandwidth = $0.5 \times F_O$	78	81.5		dB
Total Harmonic Distortion ^{3,4}	2.5V Reference			-88	dB
Total Harmonic Distortion ^{3,4}	3V Reference			-86	dB
Spurious Free Dynamic Range ^{3,4}	2.5V Reference			-90	dB
Spurious Free Dynamic Range ^{3,4}	3V Reference			-88	dB
Unipolar Mode					
Signal to Noise ^{3,4}	Measurement Bandwidth = $0.383 \times F_O$		84		dB
Signal to Noise ^{3,4}	Measurement Bandwidth = $0.5 \times F_O$		81		dB
Total Harmonic Distortion ³			-89		dB
ANALOG INPUTS					
Full Scale Input Span	$V_{IN(+)} - V_{IN(-)}$				V
Bipolar Mode	Differential or Single Ended Input	$\pm 4/5 \times V_{REF2}$			V
Unipolar Mode	Single Ended Input	0		$8/5 \times V_{REF2}$	V
Absolute Input Voltage	$V_{IN(+)}$ and/or $V_{IN(-)}$	A_{GND}		AV_{DD}	V
Input Sampling Capacitance			2		pF
Input Sampling Rate, F_{CLKIN}				19.2	MHz
CLOCK					
CLKIN Duty Ratio		45		55	%
REFERENCE					
REF1 Output Resistance			3		k Ω
Reference Buffer					
Offset Voltage	Offset between REF1 and REF2		± 10		mV
Using Internal Reference					
REF2 Output Voltage		2.39	2.54	2.69	V
REF2 Output Voltage Drift			60		ppm/ $^{\circ}\text{C}$
Using External Reference					
REF2 Input Impedance	REF1 = AGND		4		k Ω
REF2 External Voltage Range		1.2	2.5	3.15	V
STATIC PERFORMANCE					
Resolution		16*			Bits
Differential Nonlinearity (DNL) ⁴	*Guaranteed Monotonic		± 0.5	$\pm 1^*$	LSB
Integral Nonlinearity (INL) ⁴			± 2		LSB
DC CMRR ⁴		80			dB
Offset Error					
Bipolar Mode ⁴	Differential or Single Ended i/p		± 5		mV
Unipolar Mode ⁴	Single Ended i/p		± 25		mV
Gain Error ^{4,5}			± 0.5		%FSR

SPECIFICATIONS¹

($A_{V_{DD}} = +5V \pm 5\%$; $AGND = AGND1 = AGND2 = DGND = 0V$;
 $F_{CLKIN} = 19.2 \text{ MHz}$; $REF2 = 2.5 \text{ V}$; $T_A = T_{MIN}$ to T_{MAX} ; unless otherwise noted)

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
LOGIC INPUTS (Excluding CLKIN) V_{INH} , Input High Voltage V_{INL} , Input Low Voltage		2.0		0.8	V V
CLOCK INPUT (CLKIN) V_{INH} , Input High Voltage V_{INL} , Input Low Voltage		3.8		0.4	V V
ALL LOGIC INPUTS I_{IN} , Input Current C_{IN} , Input Capacitance	$V_{IN} = 0 \text{ V to } DV_{DD}$			± 10 10	μA pF
LOGIC OUTPUTS V_{OH} , Output High Voltage V_{OL} , Output Low Voltage	$ I_{OUT} = 200 \text{ mA}$ $ I_{OUT} = 1.6 \text{ mA}$	4.0		0.4	V V
POWER SUPPLIES $A_{V_{DD}}$ I_{AVDD} DV_{DD} I_{DVDD} Power Consumption ⁶	 HALF_PWR = Logic Low HALF_PWR = Logic High HALF_PWR = Logic Low HALF_PWR = Logic High Standby Mode	4.75	 50 25 20 15	5.25 60 TBD 5.25 75 TBD 200	V mA mA V mA mA μW

NOTES

¹Operating Temperature Range is as follows: B Version: -40°C to $+85^\circ\text{C}$

²Measurement Bandwidth = $0.5 \cdot F_O$

³When using the internal reference, THD and SFDR specifications apply only to input signals above 10kHz with a 10 μF decoupling capacitor between REF2 and AGND2. At frequencies below 10kHz, THD degrades to 84 dB and SFDR degrades to 86dB.

⁴ See 'Terminology' Section

⁵Gain Error excludes Reference Error

⁶ CLKIN and digital inputs static and equal to 0 or DV_{DD}

Specifications subject to change without notice

Preset Filter, Default Filter and Post Processor Characteristics¹

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
DIGITAL FILTER RESPONSE PRESET FIR Data Output Rate StopBand Attenuation LowPass Corner Frequency Group Delay Settling Time		70	MCLK/16 $133/2 \times F_{CLKIN}$ $133/F_{CLKIN}$	MCLK/8	dB
DEFAULT FILTER 0 kHz to $F_{CLKIN}/234.1$ $F_{CLKIN}/179.4$ $F_{CLKIN}/165.5$ $F_{CLKIN}/128$ to $F_{CLKIN}/2$ Group Delay Settling Time Output Data Rate, F_O	Internal ROM FIR Filter	-3 -6	TBD TBD $F_{CLKIN}/32$	± 0.001 -120	dB dB dB dB
POST PROCESSOR CHARACTERISTICS Input Data Rate Coefficient Precision Arithmetic Precision No. of Taps Permitted Decimation Factor No. of Decimation Stages Output Data Rate		2 1 MCLK/256	24 30	MCLK/8 108 256 5 MCLK/16	Bits Bits

NOTES

¹These characteristics are fixed by the design.

TIMING SPECIFICATIONS

(AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND = DGND = 0 V, REF2 = +2.5 V unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
CLKIN Frequency	f _{CLK}	1		20	MHz
CLKIN Period (t _{CLK} = 1/f _{CLK})	t ₁	0.05		1	μs
CLKIN Low Pulsewidth	t ₂	0.45 x t ₁		0.55 x t ₁	
CLKIN High Pulsewidth	t ₃	0.45 x t ₁		0.55 x t ₁	
CLKIN Rise Time	t ₄	5			ns
CLKIN Fall Time	t ₅	5			ns
CLKIN to SCO Delay	t ₆		25	40	ns
SCO Period: SCR = 0	t ₇		1		t _{CLK}
SCR = 1	t ₇		2		t _{CLK}
Serial Interface (DSP Mode Only)					
FSI Setup Time Before SCO Transition	t ₈	20			ns
FSI Hold Time After SCO Transition	t ₉	0			ns
SDI Setup Time	t ₁₀	20			ns
SDI Hold Time	t ₁₁	0			ns
Serial Interface (DSP and BFR Modes)					
SCO Transition to FSO High Delay	t ₁₂	5		10	ns
SCO Transition to FSO Low Delay	t ₁₃	5		10	ns
SDO Setup Before SCO Transition	t ₁₄	5		10	ns
SDO Hold After SCO Transition	t ₁₅	5		10	ns
Serial Interface (EPROM Mode)					
SCO High Time	t ₁₆			8	t _{CLK}
SCO Low Time	t ₁₇			8	t _{CLK}
SOE Low to First SCO Rising Edge	t ₁₈			20	t _{CLK}
Data Setup Before SCO Rising Edge	t ₁₉	10			ns
Parallel Interface					
Data Write					
RS Low to CS Low	t ₂₀	10			ns
WR Setup Before CS Low	t ₂₁	10			ns
RS Hold After CS Rising Edge	t ₂₂	10			ns
CS Pulse Width	t ₂₃	50			ns
WR Hold After CS Rising Edge	t ₂₄	10			ns
Data Setup time	t ₂₅	10			ns
Data Hold Time	t ₂₆	0			ns
Data Read					
RS Low to CS Low	t ₂₇	10			ns
RD Setup Before CS Low	t ₂₈	10			ns
RS Hold After CS Rising Edge	t ₂₉	10			ns
RD Hold After CS Rising Edge	t ₃₀	10			ns
Data Valid After CS Falling Edge	t ₃₁			25	ns
Data Hold After CS Rising Edge	t ₃₂	5			ns
Status Read/Instruction Write					
CS Duty Cycle	t ₃₃	1			t _{CLK}
Interrupt Clear After CS Low	t ₃₄			5	ns
RD Setup to CS Low	t ₃₅	10			ns
RD Hold After CS Rising Edge	t ₃₆			10	ns
Read Data Access Time	t ₃₇			25	ns
Read Data Hold After CS Rising Edge	t ₃₈	10			ns
Write Data Setup Before CS Rising Edge	t ₃₉	10			ns
Write Data Hold After CS Rising Edge	t ₄₀	5			ns

NOTE

Guaranteed by design.

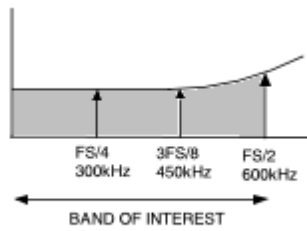


Figure 1 shows the noise floor for the AD7725. Using a 19.2MHz serial clock, the noise floor is flat up to 460kHz and begins to rise slightly from 460kHz to 600kHz. Above 600kHz the noise floor rises sharply. The usable bandwidth is therefore 600kHz (i.e. FS/2).

Figure 1. Noise Analysis

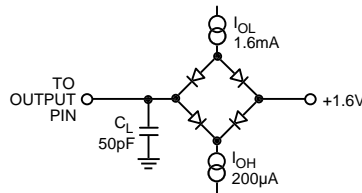


Figure 2. Load Circuit for Timing Specifications

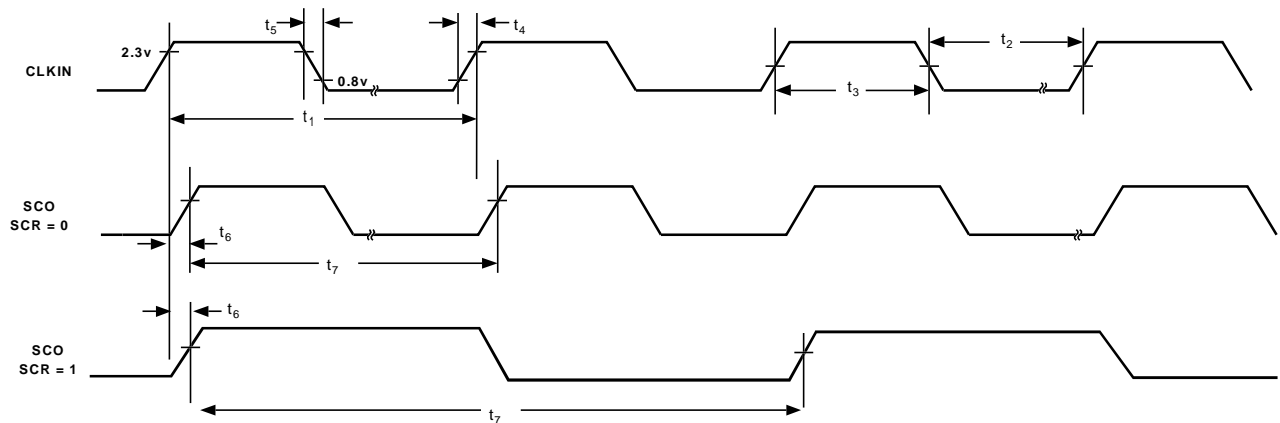


Figure 3. CLKIN to SCO Relationship.

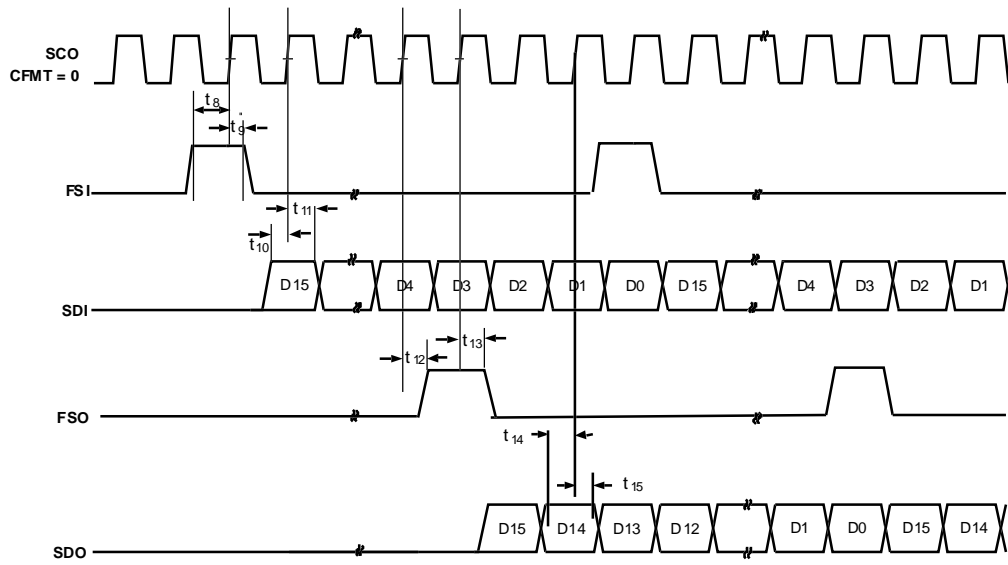


Figure 4. Serial Mode (DSP Mode and ROM mode). In ROM mode, FSI and SDI are not used.

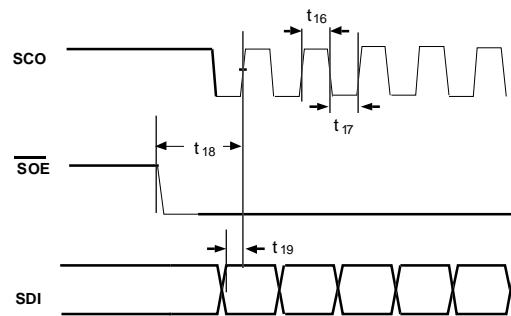


Figure 5. Serial Mode (EEPROM Mode).

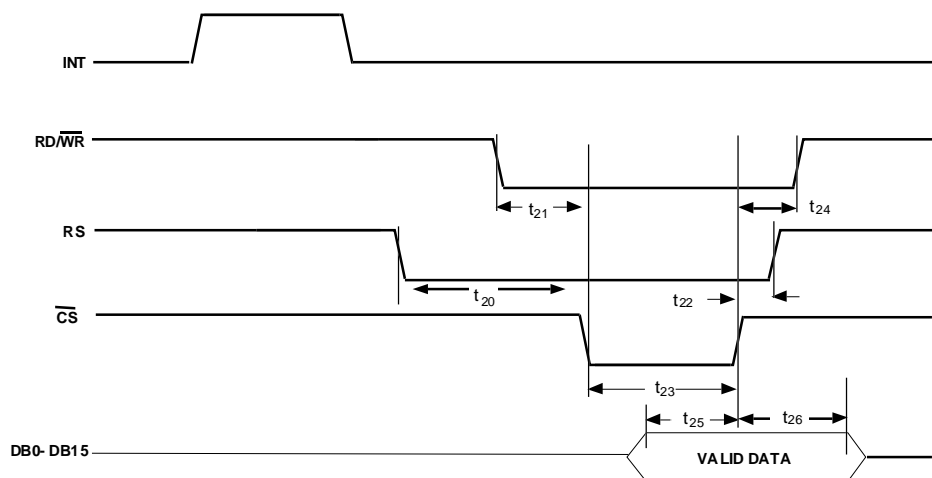


Figure 6. Parallel Mode (Writing Data to the AD7725).

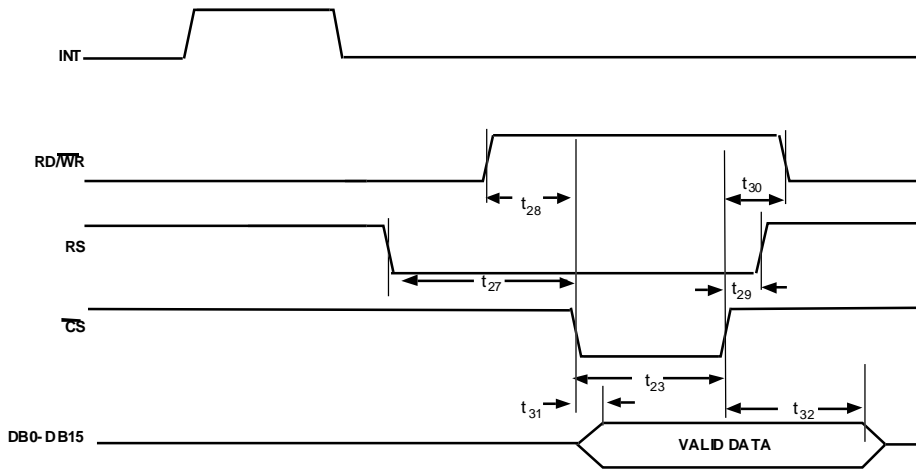


Figure 7. Parallel Mode (Reading Data from the AD7725).

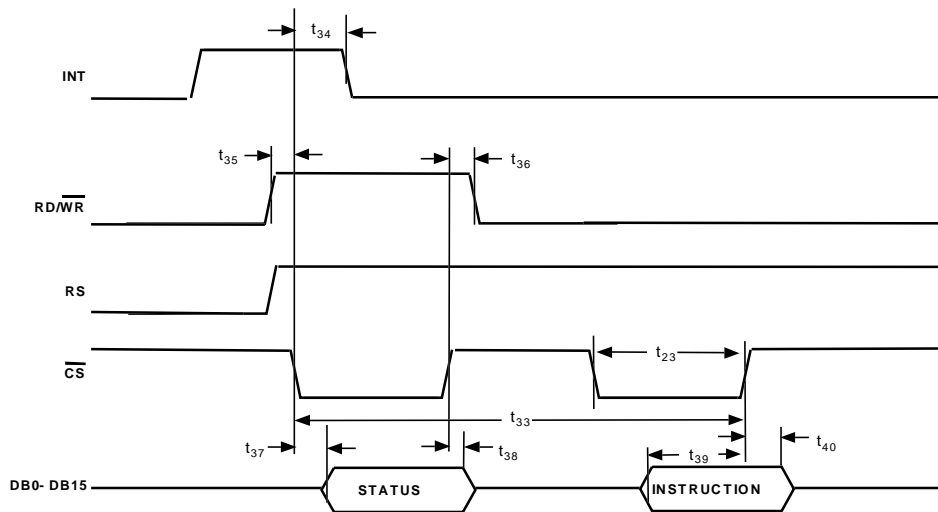


Figure 8. Parallel Mode (Reading the Status Register and Writing Instructions).

TABLE 1: PROGRAMMING MODES

S/ \bar{P}	SMODE[1, 0]	Configuration Mode	Description
0	xx	MICRO	Parallel Interface. The 16-bit Bi-Directional Microprocessor Interface is used for Read/Write Operations.
1	00	BFR	Serial Interface. Boot from the Default Filter (Internal ROM) at power on Reset (POR).
1	01	DSP	Serial Interface. Bi-Directional Serial Synchronous Interface Suitable for Interfacing to a DSP.
1	10	EEPROM	Serial Interface. Boot from external serial EPROM at POR.
1	11	"	"

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C Unless Otherwise Noted)

DV _{DD} to D _{GND}	-0.3 V to 7 V
AV _{DD} to A _{GND}	-0.3 V to 7 V
AV _{DD} , AV _{DD1} to DV _{DD}	-1 V to +1 V
AGND, AGND1 to DGND	-0.3 V to +0.3 V
Digital Inputs to DGND	-0.3 V to DV _{DD} + 0.3 V
Digital Outputs to DGND	-0.3 V to DV _{DD} + 0.3 V
V _{IN} (+), V _{IN} (-) to AGND	-0.3 V to AV _{DD} + 0.3V
REF1 to AGND	-0.3 V to AV _{DD} + 0.3V
REF2 to AGND	-0.3 V to AV _{DD} + 0.3V
REFIN to AGND	-0.3 V to AV _{DD} + 0.3V
DGND, AGND	±0.3 V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
q _{JA} Thermal Impedance	73°C/W
Lead Temperature, Soldering	
Vapor Phase(60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

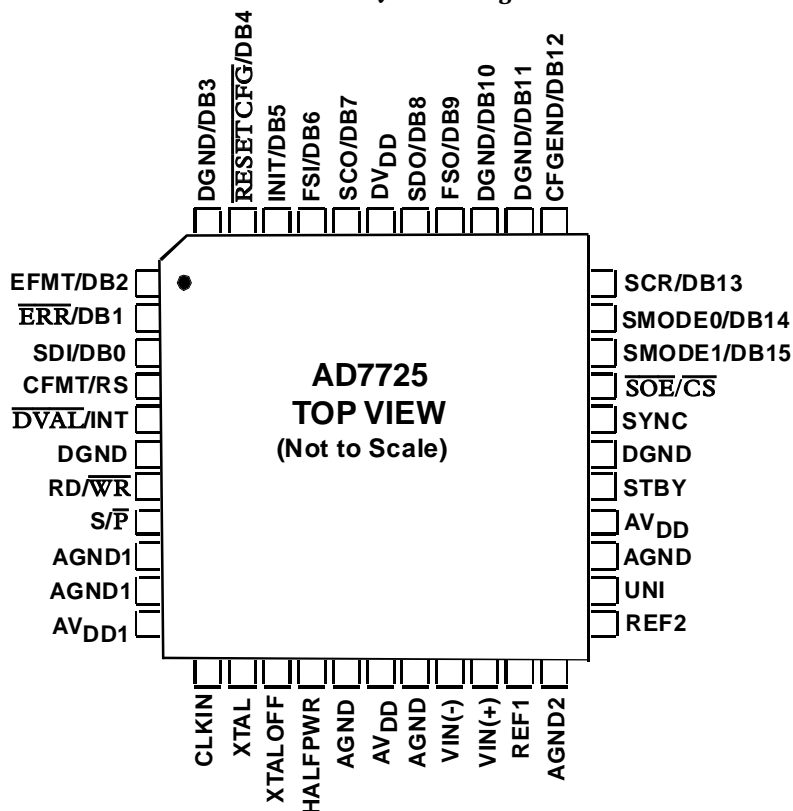
¹Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7725BS	-40°C to +85°C	S-44

*S = Plastic Quad Flatpack (PQFP).

PIN CONFIGURATION 44-Pin PQFP Package



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7725 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic S/ \bar{P}	Description
1	EFMT/DB2	Serial Mode. EFMT - Serial Clock Format, Logic Input. This clock format pin selects the clock edge to be used during configuration. When EFMT is low, Serial Data In will be valid on the rising edge of SCO and when EFMT is high, Serial Data In will be valid on the falling edge of SCO. During normal operation, this pin is ignored. Parallel Mode. DB2 - Data Output Bit.
2	$\overline{\text{ERR}}$ /DB1	Serial Mode. $\overline{\text{ERR}}$ - Configuration Error Flag, Logic Output. If an error occurs during configuration, this open collector output goes low. Parallel Mode. DB1 - Data Output Bit.
3	SDI/DB0	Serial Mode. SDI - Serial Data Input. The serial data is shifted in MSB first, in two's complement format, synchronous with SCO. Parallel Mode. DB0 - Data Output Bit (LSB).
4	CFMT/RS	Serial Mode. CFMT - Serial Clock Format, Logic Input. This clock format pin selects the clock edge to be used during normal operation. When CFMT is low, Serial Data Out is valid on the rising edge of SCO and when CFMT is high, Serial Data Out is valid on the falling edge of SCO. During configuration, this pin is ignored. Parallel Mode. RS - Register Select. RS selects between the data register, used to read conversion data or write configuration data, and the instruction register. When RS is high, the Status Register can be read or an instruction can be written to the AD7725. When RS is low, data such as the configuration file can be written to the ADC while data such as the device ID or a conversion result can be read from the AD7725 (see table 2).
5	$\overline{\text{DVAL}}$ /INT	Serial Mode. $\overline{\text{DVAL}}$ - Data Valid Logic Output. This output is low when there are no overflows in the post processor and goes high when an overflow occurs in the post processor. Parallel Mode. INT - Interrupt Logic Output. INT idles low. A logic high on this output pin indicates that user intervention is required. There are several cases when this may occur: (i) An instruction is completed. Writing an instruction or reading the status register clears the interrupt. (ii) Write data is requested. Writing data clears the interrupt. (iii) Read data is ready. Reading data clears the interrupt. (iv) An error occurs - ID or CRC error in the configuration file format, or an overflow in the post processor. Reading the Status Register clears the interrupt (v) The device completes power on reset. Reading the Status Register clears the interrupt.
6	DGND	Ground Reference for Digital Circuitry.
7	RD/ $\overline{\text{WR}}$	Parallel Mode. Read/Write Logic Input. A read cycle is initiated when RD/ $\overline{\text{WR}}$ is high. A write cycle is initiated when RD/ $\overline{\text{WR}}$ is low.
8	S/ \bar{P}	Serial/Parallel Interface Select. When S/ \bar{P} is tied low, parallel mode is selected. Serial mode is selected when S/ \bar{P} is tied high. The modes cannot be altered dynamically.
9	AGND1	Digital Logic Power Supply Ground for the Analog Modulator.
10	AGND1	Digital Logic Power Supply Ground for the Analog Modulator.
11	AV _{DD1}	Digital Logic Power Supply for the Analog Modulator.
12	CLKIN	Clock Input. An external clock source can be applied directly to this pin with XTAL_OFF tied high. Alternatively, a parallel resonant fundamental frequency crystal, in parallel with a 1 M Ω resistor can be connected between the XTAL pin and the CLKIN pin with XTAL_OFF tied low. External capacitors are then required from the CLKIN and XTAL pins to ground. Consult the crystal manufacturer's recommendation for the load capacitors.
13	XTAL	Input to Crystal Oscillator Amplifier. If an external clock is used, XTAL should be tied to AGND1.
14	XTALOFF	Oscillator Enable Input. A logic high disables the crystal oscillator amplifier to allow use of an external clock source. Set low when using an external crystal between the CLKIN and XTAL pins.
15	HALF_PWR	Logic Input. When set high, the power dissipation is reduced by approximately one half and a maximum CLKIN frequency of 10 MHz applies.

PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic S/ \bar{P}	Description
16	AGND	Power Supply Ground for the Analog Modulator.
17	AV _{DD}	Positive Power Supply Voltage for the Analog Modulator.
18	AGND	Power Supply Ground for the Analog Modulator.
19	V _{IN} (-)	Negative Terminal of the Differential Analog Input.
20	V _{IN} (+)	Positive Terminal of the Differential Analog Input.
21	REF1	Reference Output. REF1 connects through 3k Ω to the output of the internal 2.5 V reference and to a buffer amplifier that drives the Σ - Δ modulator.
22	AGND2	Power Supply Ground return to the Reference Circuitry, REF2, of the Analog Modulator.
23	REF2	Reference Input. REF2 connects to the output of an external buffer amplifier used to drive the Σ - Δ modulator. When REF2 is used as an input, REF1 must be connected to AGND to disable the internal buffer amplifier.
24	UNI	Analog Input Range Select Input. The UNI pin selects the analog input range for either bipolar (differential or single ended input) or unipolar (single ended input) operation. A logic high input selects unipolar operation and a logic low selects bipolar operation.
25	AGND	Power Supply Ground for the Analog Modulator.
26	AV _{DD}	Positive Power Supply Voltage for the Analog Modulator.
27	STBY	Standby, Logic Input. When STBY is taken high, the device will enter a low power mode. If the device was fully configured before entering this mode, it will not lose its configuration data. When STBY is brought low, the device exits the low power mode. If the device was partly configured before entering the low power mode, it will restart the configuration process in the case of BFR mode and EEPROM mode or, in parallel mode, a new configure instruction must be issued to configure the device. If the device was fully configured before entering the low power mode, it will continue to output conversion results in all serial modes and in parallel mode, the device will wait for an instruction to begin converting.
28	DGND	Ground Reference for Digital Circuitry.
29	SYNC	Synchronization Logic Input. When using more than one AD7725, operated from a common master clock, SYNC allows each ADC to simultaneously sample its analog input and update its output register. When SYNC is high, the digital filter sequencer counter is reset to zero and the post processor core is reset. Because the digital filter and sequencer are completely reset during this action, SYNC pulses cannot be applied continuously. When SYNC is taken low, normal conversion continues.
30	$\overline{SOE}/\overline{CS}$	Serial Mode. SOE - Serial Output Enable. \overline{SOE} enables the external EPROM and is used to reset the EEPROM's address counter. In DSP mode, \overline{SOE} is an active high interrupt. It goes high after power on reset, indicating the device is ready to be configured and after configuration, indicating the device was configured correctly. In both cases, \overline{SOE} is reset low when FSI is detected high by CLKIN. In BFR mode, \overline{SOE} pulses high for 8 CLKIN cycles at the end of a successful configuration Parallel Mode. \overline{CS} - Chip Select Logic Input. This is a positive edge trigger used to complete a read/write cycle.
31	SMODE1/DB15	Serial Mode. SMODE1 - Serial Mode Select, Logic Input. This pin selects the serial mode to be used (see table 1) and thus informs the device where to download configuration data from automatically on power up. The value on this input cannot be altered dynamically.
32	SMODE0/DB14	Parallel Mode. DB15 - Data Output Bit (MSB). Serial Mode. SMODE0 - Serial Mode Select, Logic Input. This pin selects the serial mode to be used (see table 1) and thus informs the device where to download configuration data from automatically on power up. The value on this input cannot be altered dynamically. Parallel Mode. DB14 - Data Output Bit.

PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic S/ \bar{P}	Description
33	SCR/DB13	Serial Mode. SCR - Serial Clock Rate Select, Logic Input. With SCR set to logic low, the serial clock output frequency, SCO, is equal to the CLKIN frequency. A logic high sets the frequency of SCO to one half the CLKIN frequency. Parallel Mode. DB13 - Data Output Bit.
34	CFGEND/DB12	Serial Mode. CFGEND - Configuration End, Logic Output. A logic high on CFGEND indicates that device programming is complete and no programming errors occurred. Parallel Mode. DB12 - Data Output Bit.
35	DGND/DB11	Serial Mode. DGND - Digital Ground. Parallel Mode. DB11 - Data Output Bit.
36	DGND/DB10	Serial Mode. DGND - Digital Ground. Parallel Mode. DB10 - Data Output Bit.
37	FSO/DB9	Serial Mode. FSO - Frame Synchronization Output. FSO indicates the beginning of a word transmission on the SDO pin. The FSO signal is a positive pulse approximately one SCO period wide. Parallel Mode. DB9 - Data Output Bit.
38	SDO/DB8	Serial Mode. SDO - Serial Data Output. The serial data is shifted out MSB first, in two's complement format, synchronous with SCO. Parallel Mode. DB8 - Data Output Bit.
39	DV _{DD}	Digital Power Supply Voltage.
40	SCO/DB7	Serial Mode. SCO - Serial Clock Output. The frequency is set by the SCR pin. Parallel Mode. DB7 - Data Output Bit.
41	FSI/DB6	Serial Mode. FSI - Frame Synchronization Input. FSI indicates the beginning of a word on the SDI pin. Parallel Mode. DB6 - Data Output Bit.
42	INIT/DB5	Serial Mode. INIT - Logic Input. When the device is correctly configured, a logic low on this pin will prevent the device from converting. When this pin is taken high, the device will start converting. When daisy chaining multiple devices, this pin ensures that all devices sample their analog inputs simultaneously without needing to activate the SYNC pin. Parallel Mode. DB5 - Data Output Bit.
43	$\overline{\text{RESETCFG}}$ /DB4	Serial Mode. RESETCFG - Logic Input. $\overline{\text{RESETCFG}}$ is used to reset the part when a configuration error occurs. A low pulse on this pin will reset the part and the configuration file will be downloaded again. Parallel Mode. DB4 - Data Output Bit.
44	DGND/DB3	Serial Mode. DGND - Digital Ground. Parallel Mode. DB3 - Data Output Bit.

TERMINOLOGY

Integral Nonlinearity (INL)

This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (100...00 to 100...01 in bipolar mode, 000...00 to 000...01 in unipolar mode) and full scale, a point 0.5 LSB above the last code transition (011...10 to 011...11 in bipolar mode, 111...10 to 111...11 in unipolar mode). The error is expressed in LSBs.

Differential Nonlinearity (DNL)

This is the difference between the measured and the ideal 1 LSB change between two adjacent codes in the ADC.

Common Mode Rejection Ratio (CMRR)

The ability of a device to reject the effect of a voltage applied to both input terminals simultaneously—often through variation of a ground level—is specified as a common-mode rejection ratio. CMRR is the ratio of gain for the differential signal to the gain for the common-mode signal.

Unipolar Offset Error

Unipolar offset error is the deviation of the first code transition from the ideal $V_{IN(+)}$ voltage which is ($V_{IN(-)} + 0.5$ LSB) when operating in the unipolar mode.

Bipolar Offset Error

This is the deviation of the midscale transition code (111...11 to 000...00) from the ideal $V_{IN(+)}$ voltage which is ($V_{IN(-)} - 0.5$ LSB) when operating in the bipolar mode.

Gain Error

The first code transition should occur at an analog value 0.5 LSB above negative full scale. The last transition should occur for an analog value 1.5 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-(Noise + Distortion)

Signal to (Noise + Distortion) is the measured signal-to-noise plus distortion ratio at the output of the ADC. The signal is the RMS magnitude of the fundamental. Noise plus distortion is the rms sum of all of the nonfundamental signals and harmonics up to half the Output Data Rate ($F_O/2$), excluding dc. Signal to (Noise + Distortion) is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical Signal to (Noise + Distortion) ratio for a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02N + 1.76) \text{ dB}$$

where N is the number of bits.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the harmonics to the rms value of the fundamental. THD is defined as:

$$\text{THD} = 20 \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \right)$$

where V_1 is the rms amplitude of the fundamental and V_2 , V_3 , V_4 , V_5 , and V_6 are the rms amplitudes of the second through sixth harmonics.

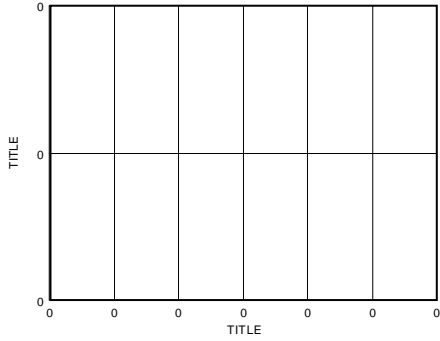
Spurious Free Dynamic Range (SFDR)

Defined as the difference, in dB, between the peak spurious or harmonic component in the ADC output spectrum (up to $F_O/2$ and excluding dc) and the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the output spectrum of the FFT. For input signals whose second harmonics occur in the stop band region of the digital filter, the spur in the noise floor limits the SFDR.

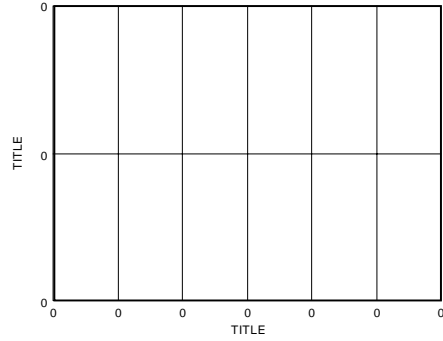
AD7725

PERFORMANCE PLOTS

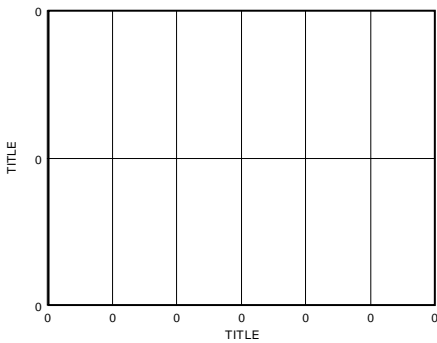
The following typical plots are generated using the default filter stored in internal ROM. This filter gives an output data rate of 600kHz (total decimate by 32), a cut off frequency of 82kHz and a stopband frequency of 150kHz.



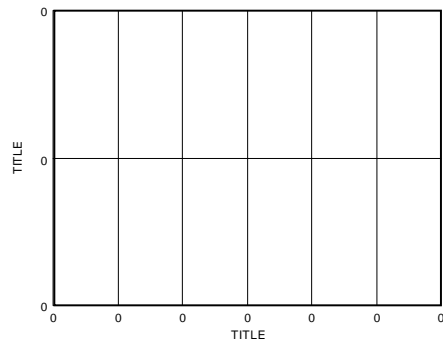
TPC 1. SNR, THD and SFDR vs. Analog Input Level Relative to Full Scale



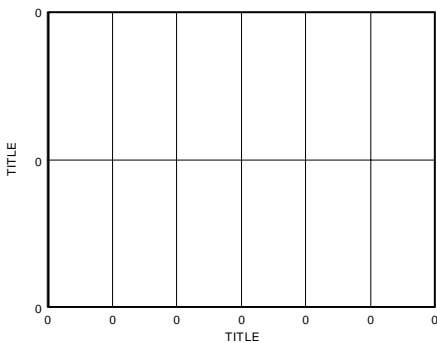
TPC 4. Histogram of Output Codes for a DC input



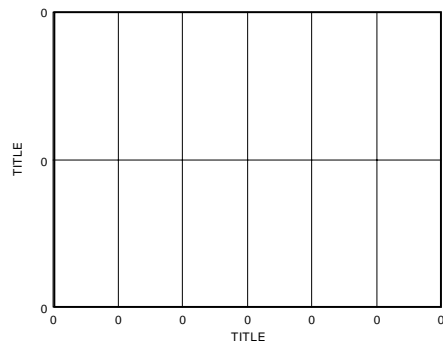
TPC 2. SNR, THD and SFDR vs. Sampling Frequency



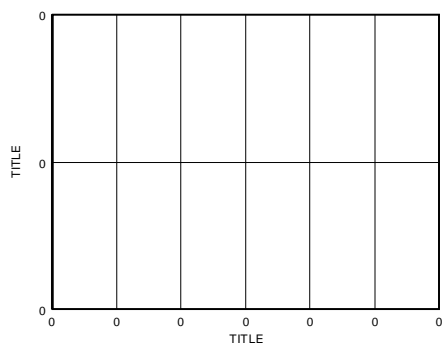
TPC 5. Power Consumption vs. CLKIN Frequency



TPC 3. SNR and THD vs. Temperature

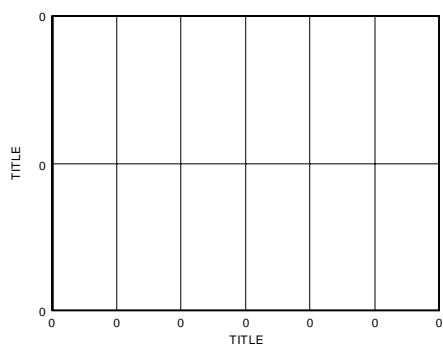


TPC 6. 16K Point FFT

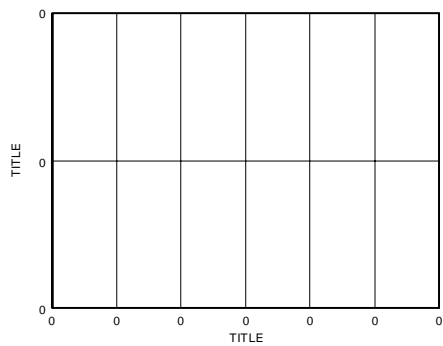


TPC 7. Modulator Output

TPC 8 and 9 show FFTs for externally designed filters downloaded into the post processor.



TPC 8. FFT for TBDkHz Low Pass Filter



TPC 9. FFT for TBDkHz Low Pass Filter

CIRCUIT DESCRIPTION

The AD7725 employs a sigma-delta conversion technique to convert the analog input into an equivalent digital word. The modulator samples the input waveform and outputs an equivalent digital word at the input clock frequency, f_{CLKIN} .

Due to the high oversampling rate, which spreads the quantization noise from 0 to $f_{CLKIN}/2$, the noise energy contained in the band of interest is reduced (Figure 9a). To further reduce the quantization noise, a high order modulator is employed to shape the noise spectrum, so that most of the noise energy is shifted out of the band of interest (Figure 9b).

The digital filter which follows the modulator removes the large out-of-band quantization noise (Figure 9c) while also reducing the data rate from f_{CLKIN} at the input of the filter to $f_{CLKIN}/16$ or less at the output of the filter, depending on the filter type used.

Digital filtering has certain advantages over analog filtering. Since digital filtering occurs after the A/D conversion, it can remove noise injected during the conversion process. Analog filtering cannot do this. The digital filter also has a linear phase response.

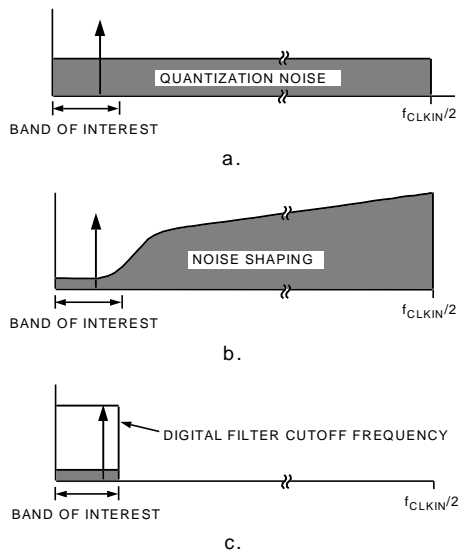


Figure 9. Sigma-Delta ADC

The AD7725 employs three fixed Finite Impulse Response (FIR) filters in series. Each individual filter's output data rate is half that of the filter's input data rate. The fourth stage is programmable, the user being able to select a lowpass, bandpass, stopband or highpass filter response. Both the filter response and the decimation are user programmable.

APPLYING THE AD7725

Analog Input Range

The AD7725 has differential inputs to provide common-mode noise rejection. In unipolar mode, the analog input is single ended and its range is 0 to $(8/5 \times V_{REF2})$. In bipolar mode, the analog input is single-ended or differential and its input range is $\pm(4/5 \times V_{REF2})$. The output code is two's complement binary in both modes with 1 LSB = $61\mu V$.

The ideal input/output transfer characteristics for the two modes are shown in Figure 10. In both modes, the absolute voltage on each input must remain within the supply range AGND to AV_{DD} . The bipolar mode allows either single-ended or differential input signals while the unipolar mode allows single-ended signals.

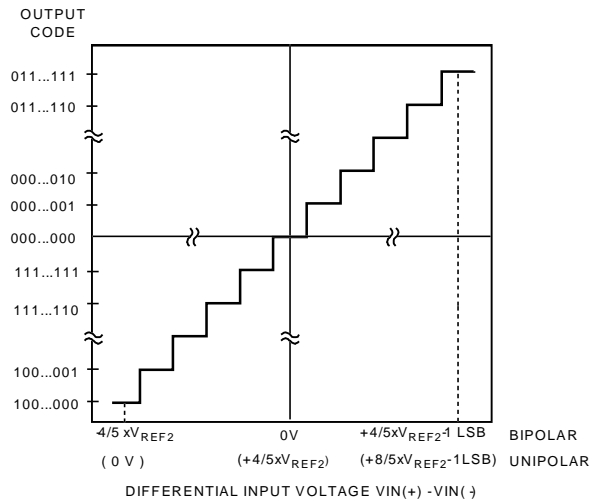


Figure 10. Bipolar (Unipolar) Mode Transfer Function

The AD7725 will accept fullscale inband signals. However, large scale out-of-band signals can overload the modulator inputs. A minimal single-pole RC antialias filter set to $f_{CLKIN}/24$ will allow fullscale input signals over the entire frequency spectrum.

Analog Input

The analog input of the AD7725 uses a switched capacitor technique to sample the input signal. For the purpose of driving the AD7725, an equivalent circuit of the analog inputs is shown in Figure 11. For each half clock cycle, two highly linear sampling capacitors are switched to both inputs, converting the input signal into an equivalent sampled charge. A signal source driving the analog inputs must be able to source this charge, while also settling to the required accuracy by the end of each half-clock phase.

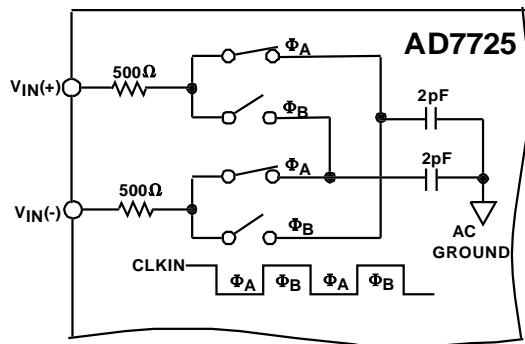


Figure 11. Analog Input Equivalent Circuit

Driving the Analog Inputs

To interface the signal source to the AD7725, at least one op amp will generally be required. The choice of op amp will be critical to achieving the full performance of the AD7725. The op amp not only has to recover from the transient loads that the ADC imposes on it but, must also have good distortion characteristics and very low input noise. Resistors in the signal path will also add to the overall thermal noise floor, necessitating the choice of low value resistors.

Placing an RC filter between the drive source and the ADC inputs, as shown in Figure 12, has a number of beneficial affects: transients on the op amp outputs are significantly reduced since the external capacitor now supplies the instantaneous charge required when the sampling capacitors are switched to the ADC input pins and, input circuit noise at the sample images is now significantly attenuated resulting in improved overall SNR. The external resistor serves to isolate the external capacitor from the ADC output, thus improving op amp stability while also isolating the op amp output from any remaining transients on the capacitor. By experimenting with different filter values, the optimum performance can be achieved for each application. As a guideline, the RC time constant ($R \times C$) should be less than a quarter of the clock period to avoid nonlinear currents from the ADC inputs being stored on the external capacitor and degrading distortion. This restriction means that this filter cannot form the main antialias filter for the ADC.

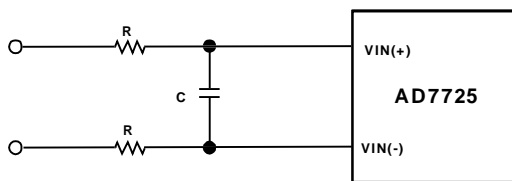


Figure 12. Input RC Network

With the unipolar input mode selected, just one op amp is required to buffer the single-ended input signal to the $V_{IN}(+)$ input and a dc input is applied to the $V_{IN}(-)$ pin to provide an offset. However, driving the AD7725 with differential signals (i.e. the bipolar input range is selected) has some distinct advantages: even order harmonics in both the drive circuits and the AD7725 front end are attenuated; and the peak to peak input signal range on both inputs is halved. Halving the input signal range allows some op amps to be powered from the same supplies as the AD7725. An example of providing differential drive to the AD7725 is to use a dual opamp.

Dual Opamp

Although this differential drive circuit will require the use of two op amps per ADC, it may avoid the need to generate additional supplies just for these op amps.

Figure 13 and 14 show two such circuits for driving the AD7725. Figure 13 is intended for use when the input signal is biased about 2.5 V while Figure 14 is used when the input signal is biased about ground. While both circuits convert the input signal into a differential signal, the circuit in Figure 14 also level shifts the signal so that both outputs are biased about 2.5 V.

Suitable op amps include the AD8047, AD8044, AD8041 and its dual equivalent the AD8042 or the AD8022. The AD8047 has lower input noise than the AD8041/42 but has to be supplied from a +7.5 V/-2.5 V supply. The AD8041/AD8042 will typically degrade the SNR from 90 dB to 80 dB but can be powered from the same single 5 V supply as the AD7725.

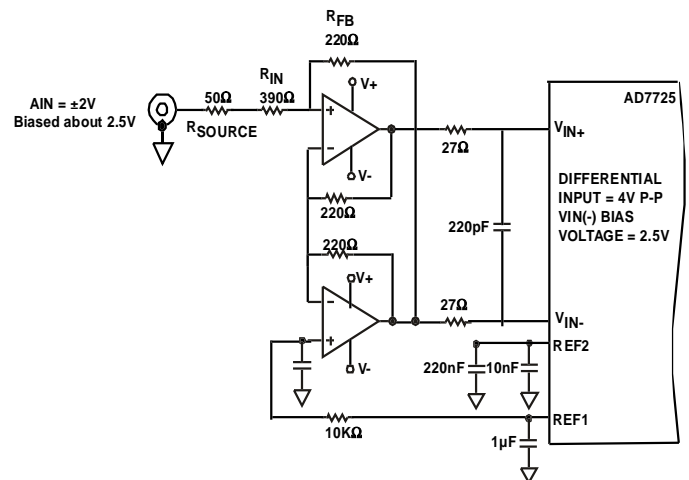
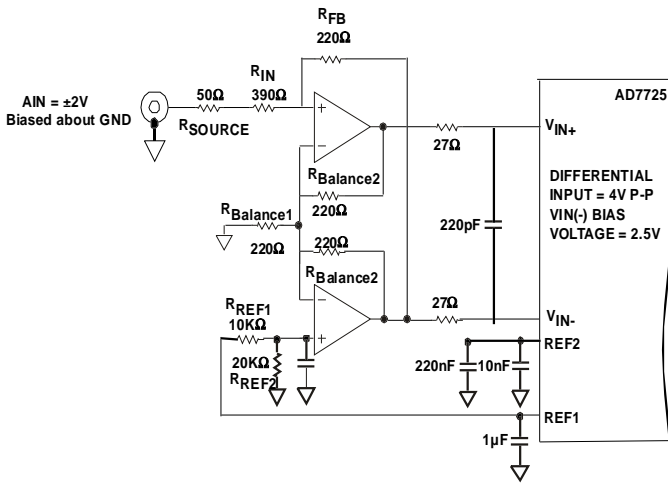


Figure 13. Single-Ended to Differential Input Circuit for Bipolar Mode Operation (Analog Input Biased About +2.5V)



$$\text{GAIN} = 2 \times R_{FB} / (R_{IN} + R_{SOURCE})$$

$$R_{Balance1} = R_{Balance2} \times (R_{IN} + R_{SOURCE}) / (2 \times R_{FB})$$

$$R_{REF2} = R_{REF1} \times (R_{IN} + R_{SOURCE}) / R_{FB}$$

Figure 14. Single-Ended to Differential Input Circuit for Bipolar Mode Operation (Analog Input Biased About Ground)

Applying the Reference

The reference circuitry used in the AD7725 includes an on chip 2.5 V bandgap reference and a reference buffer circuit. The block diagram of the reference circuit is shown in Figure 15. The internal reference voltage is connected to REF1 through a 3 kΩ resistor and is internally buffered to drive the analog modulator's switched cap DAC (REF2). When using the internal reference, a 1μF capacitor is required between REF1 and AGND to decouple the bandgap noise. If the internal reference is required to bias external circuits, use an external precision op amp to buffer REF1.

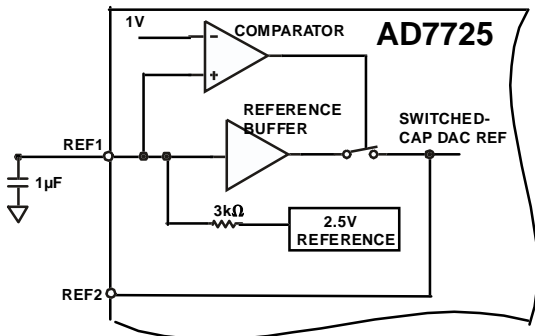


Figure 15. Reference Circuit Block Diagram

Where gain error or gain drift requires the use of an external reference, the reference buffer in Figure 16 can be turned off by grounding the REF1 pin and the external

reference can be applied directly to pin REF2. The AD7725 will accept an external reference voltage between 1.2 V and 3.15 V. By applying a 3 V rather than a 2.5 V reference, SNR is typically improved by about 1 dB.

Where the output common-mode range of the amplifier driving the inputs is restricted, the fullscale input signal span can be reduced by applying a lower than 2.5 V reference. For example, a 1.25 V reference would make the bipolar (differential) input range ±1 V but would degrade SNR.

In all cases, since the REF2 voltage connects to the analog modulator, a 220 nF and 10 nF capacitor must connect directly from REF2 to AGND. The external capacitor provides the charge required for the dynamic load presented at the REF2 pin (see Figure 16).

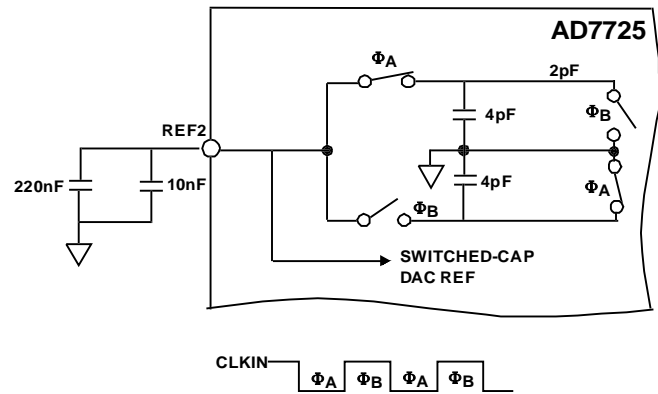


Figure 16. REF2 Equivalent Input Circuit

The AD780 is ideal to use as an external reference with the AD7725. Figure 17 shows a suggested connection diagram. Grounding pin 8 on the AD780 selects the 3 V output mode.

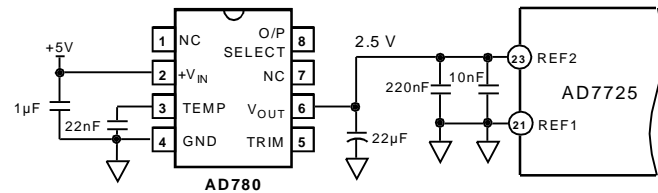


Figure 17. External Reference Circuit Connection

Clock Generation

The AD7725 contains an oscillator circuit to allow a crystal or an external clock signal to generate the master clock for the ADC. The connection diagram for use with a crystal is shown in Figure 18. Consult the manufacturer's recommendation for the load capacitors. To enable the oscillator circuit on board the AD7725, XTAL_OFF should be tied low.

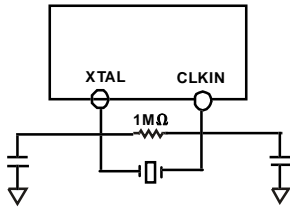


Figure 18. Crystal Oscillator Connection

When an external clock source is being used, the internal oscillator circuit can be disabled by tying XTAL_OFF high. A low phase noise clock should be used to generate the ADC sampling clock because sampling clock jitter effectively modulates the input signal and raises the noise floor. The sampling clock generator should be isolated from noisy digital circuits, grounded and heavily decoupled to the analog ground plane.

The sampling clock generator should be referenced to the analog ground in a split ground system. However, this is not always possible because of system constraints. In many applications, the sampling clock must be derived from a higher frequency multi-purpose system clock that is generated on the digital ground plane. If the clock signal is passed between its origin on a digital ground plane to the AD7725 on the analog ground plane, the ground noise between the two planes adds directly to the clock and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling signal as a differential one, using either a small RF transformer or a high speed differential driver and a receiver such as PECL. In either case, the original master system clock should be generated from a low phase noise crystal oscillator.

SYSTEM SYNCHRONIZATION

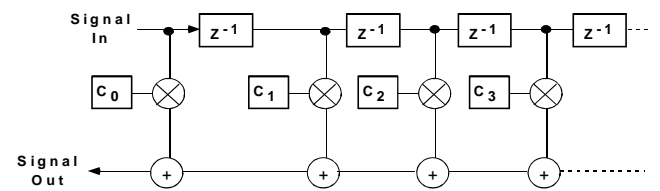
The SYNC input provides a synchronization function for use in parallel or serial mode. SYNC allows the user to begin gathering samples of the analog input from a known point in time. This allows a system using multiple AD7725s, operated from a common master clock, to be synchronized so that each ADC simultaneously updates its output register. In a system using multiple AD7725s, a common signal to their SYNC inputs will synchronize their operation. When SYNC is high, the digital filter sequencer is reset to zero. A SYNC pulse, one CLKIN cycle long, can be applied. This way, SYNC is sensed low on the next rising edge of CLKIN. When SYNC is sensed low, normal conversion continues. Following a SYNC, the modulator and filter need time to settle before data can be read from the AD7725. Also, when INIT is taken high, it activates SYNC, which ensures that multiple devices cascaded in serial mode will sample their analog inputs simultaneously.

POST PROCESSOR

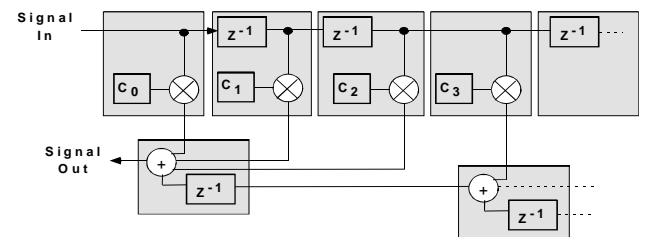
The AD7725 contains Systolix's PulseDSP* post processor. The post processor core is a systolic array of simple high performance processors. There are 108 of these in the AD7725. In a systolic array, data is pumped between

processors. Each of these processors is allocated to a dedicated function and will only perform that single function. The data is passed between processors and, in this manner, complex operations are performed on the signal. Figure 19 shows an example of a filtering function implemented on the post processor. Figure 19a shows the data path representation of an FIR filter while figure 19b shows how this algorithm would be implemented on the AD7725. It can be seen from this example that a single FIR tap requires 1.3 processors for implementation. This is a useful guideline when calculating the design requirements for a new application. In the AD7725, data transfers between processors are fully synchronous. As a result, the user does not have to consider timing issues.

*PulseDSP is a trademark of Systolix



a) FIR Data Path Representation



b) FIR Post Processor Implementation

Figure 19. AD7725 Processor Mapping

The processor core is optimised for signal conditioning applications. In this type of application, the most common function is generally filtering. The core can support any filter structure, whether FIR, IIR, recursive or non-recursive. As can be seen from the previous example, this type of algorithm maps very efficiently to the post processor. The core also supports polynomial functions, commonly used in linearisation algorithms.

Data can be transparently decimated or interpolated when passed between processors. This simplifies the design of multi-rate filtering and gives great flexibility when specifying the final output word rate. The AD7725 post processor supports decimation/interpolation by factors up to 256.

To program the post processor, the user must produce a configuration file which contains the programming data for the intended function or load the internal default filter into the post processor. The configuration file can be generated by a digital filter design package called 'Filter Wizard' which is available from Systolix (www.systolix.co.uk). This package allows the user to

AD7725

design different filter types and generates the appropriate configuration file to be downloaded into the postprocessor.

The post processor holds 8064 bits of data. A configuration file loaded into the post processor must therefore contain exactly 8064 bits. The data is split into blocks of 672 bits in the configuration file. The AD7725 accepts 672 bits of data and checks it for errors. If there are no errors, the data is loaded into the post processor and the device awaits the next 672 bits of data. If the data is corrupt, the AD7725 abandons loading data into the post processor. See the Serial and Parallel Mode sections for further information on how configuration errors are detected and handled.

Internal Default Filter

The AD7725 has a default filter stored in internal ROM. This is a two stage, low pass, FIR filter with a cutoff frequency of 82kHz and a stopband frequency of 150kHz. This filter has a total decimation by four which occurs in the first stage, resulting in output data being available to the serial interface at CLKIN/32. For more detailed specifications on this filter see the 'Preset Filter, Default Filter and Post Processor Characteristics' section. When powered up in Boot-from-ROM mode, the AD7725 will automatically load the default filter characteristic into the post processor. Figure 20 shows how the post processor is programmed using the default filter and figure 21 shows the default filter response.

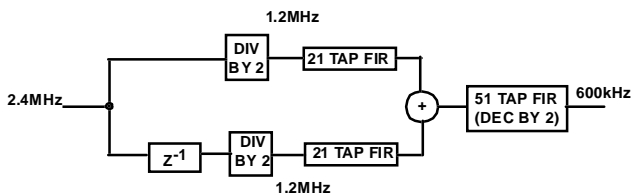


Figure 20. Default Post Processor Programming

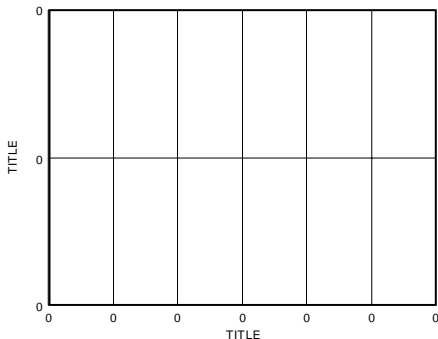


Figure 21. Default Post Processor Programming TBD

PROGRAMMING THE POST PROCESSOR

The coefficients file for the filter response can be generated using a digital filter design package such as 'Filter Wizard' from Systolix (www.systolix.co.uk). This package allows the user to design different filter types (FIR, IIR, etc) and creates the configuration files to be downloaded into the postprocessor. The response of the filter can be plotted so that the user knows the response

(cutoff frequency, rolloff, attenuation) before generating the coefficients.

When using the post processor, the data is available to the processor at 2.4 MHz. When decimation is employed, in a multi-stage filter, the first filter will be operated at 2.4 MHz and the user can then decimate between stages. The number of taps which can be contained in the post processor is 108. Therefore, a single filter with 108 taps can be generated or, a multi-stage filter can be designed whereby the total number of taps adds up to 108.

At a given filter frequency, any bandwidth requires the same number of taps. However, the number of taps increases as the filter rolloff is increased. Therefore, a filter with a bandwidth of 300 kHz which rolls off between 300 kHz and 600 kHz uses less taps than a filter with a cutoff frequency of 300 kHz which rolls off between 300 kHz and 450 kHz.

To reduce the number of taps needed, a multi-stage filter can be designed with decimation performed between stages. When decimation is performed, the noise is wrapped around the filter frequency divided by 2 each time the output is decimated by 2 so, the user needs to ensure that the quantisation noise is reduced sufficiently i.e. the quantisation noise should be filtered in a given area if this region will map into the bandwidth of interest during decimation. With appropriate filtering, the noise floor will increase by 3 dB each time that the data stream is decimated by 2. However, the noise floor is down at 120 dB prior to decimation. Therefore, with suitable decimation, the SNR will be 90 dB typically at the AD7725 output.

Although decimation causes the noise floor to increase by 3 dB each time that the data stream is decimated by 2, decimation causes a reduction in the number of filter taps needed for a given response. For example, the number of taps needed to generate a cutoff frequency of 300 kHz and a stopband frequency of 600 kHz will equal the number of taps needed to generate a filter with a cutoff frequency of 300 kHz and a stopband frequency of 450 kHz if the data stream is decimated by 2 prior to the filtering stage. However, the user must ensure that the quantisation noise has been filtered prior to this filtering stage. Otherwise, the noise floor will be increased in the bandwidth of interest and the SNR will degrade.

To generate an FIR filter with a cutoff frequency of 300 kHz, a stopband frequency of 600 kHz, a passband ripple of 0.01 dB and a stopband attenuation of 90 dB requires 47 taps when the Kaiser window is used. To generate a similar filter with a stopband frequency of 450 kHz requires 93 taps. By decimating the data stream prior to filtering, the filter frequency will equal 1.2 MHz rather than 2.4 MHz and the number of taps needed to generate this response is 47. When the filter design is complete and the configuration file has been generated it can be downloaded into the post processor.

MODES OF OPERATION (See table 1)

SERIAL MODE

The serial mode is selected by tying S/\bar{P} to V_{DD} . In this mode, there are a three 'sub-modes' which determine how the device is to be configured. These are:

(i) The default filter (Internal ROM) can be loaded into the post processor.

The filter can be user defined and it can be loaded from either (ii) a DSP or (iii) an external EPROM.

These modes are selected by the values on SMODE0 and SMODE1 (see Table 1). In serial mode, several AD7725s can be daisy-chained together so they can all be configured from one EEPROM or DSP and conversion data from all devices can be read back by one DSP.

Using the Internal Default Filter (BFR Mode)

This mode of operation is selected by tying SMODE0 and SMODE1 to ground. The values on these pins inform the AD7725 that the post processor is to be configured with the default filter stored in internal ROM. The default filter data will be loaded into the post processor automatically on power up. Once the configuration is complete, CFGEND will go high. In figure 22, CFGEND is tied to INIT thus it will drive the INIT pin high and the AD7725 will begin converting.

FSI and SDI are not used in this mode so should be hardwired to ground. In this mode of operation, the AD7725 operates as a normal sigma-delta ADC with a fixed filter response.

During configuration, SCO will have a frequency of $CLKIN/16$. Once configuration is complete, the frequency of SCO is selected by SCR and will be either $CLKIN$ or $CLKIN/2$. Additionally, the SCO edge on which the data is output from the device can be selected using CFMT.

With $SCR = 0$, SCO equals $CLKIN$. With $SCR = 1$, SCO equals $CLKIN/2$. With $CFMT = 0$, data is output on the SCO rising edge while data is output on the falling edge when $CFMT = 1$.

Figure 22 shows the connection diagram for the AD7725 when using the internal default filter and figure 23 shows a flow chart of the powerup and configuration sequence.

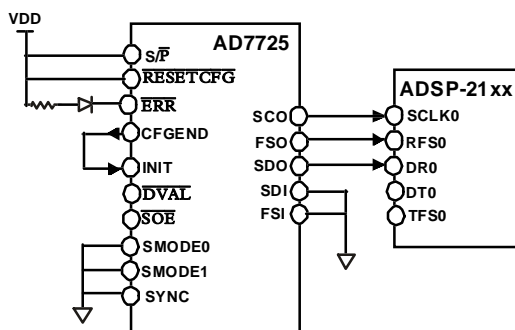


Figure 22. AD7725 using the Default Filter

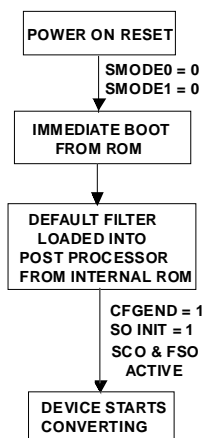


Figure 23. Flow Chart of Boot From ROM mode

Loading Configuration Data from a DSP (DSP Mode)

In this mode, a filter is developed off-chip by the user and the resulting configuration file is loaded into the post processor in the AD7725 from a DSP. The DSP therefore loads data into the AD7725 and reads back the conversion results. This mode of operation is selected by tying SMODE0 to V_{DD} and SMODE1 to ground. The values on these pins inform the AD7725 that user defined filter data is to be loaded into the post processor from the DSP automatically on powerup. The data is loaded using FSI and SDI and the transfer of data is controlled by SCO. If it is necessary to ensure that the AD7725 has completed its power on reset sequence before the DSP starts to send the configuration data, the \overline{SOE} pin can be used as an interrupt. If no errors occur during the configuration, CFGEND will go high. In figure 24, CFGEND is tied to INIT thus it will drive INIT high and the part will begin converting. However, if an error does occur during the configuration, the \overline{ERR} bit will go low and CFGEND will not go high. The INIT pin will therefore not start conversions. The part will not do anything until $\overline{RESETCFG}$ is pulsed low. When this occurs, the part is reset and the configuration file is reloaded.

Note: The AD7725 will read the entire configuration file (672 bits at a time) and if an error does occur during configuration, the user will only be notified once the whole file has been read, by the \overline{ERR} bit going low. In this case, the data will not be loaded into the post processor.

The AD7725 has a synchronous serial interface. It generates the serial clock SCO whose frequency can be $CLKIN$ ($SCR = 0$) or $CLKIN/2$ ($SCR = 1$). SCO must have a frequency equal to $CLKIN$ if the AD7725 outputs data at $CLKIN/16$. For lower output word rates, either clock frequency can be used. To load configuration data into the AD7725, an FSI pulse of one $CLKIN$ cycle wide informs the AD7725 that data is being transferred into the device. The data is loaded using the next 16 SCLK cycles following the detection of the FSI pulse. Figure 24 shows the connection diagram for the AD7725 when

AD7725

loading configuration data from a DSP and figure 25 shows a flow chart of the powerup and configuration sequence.

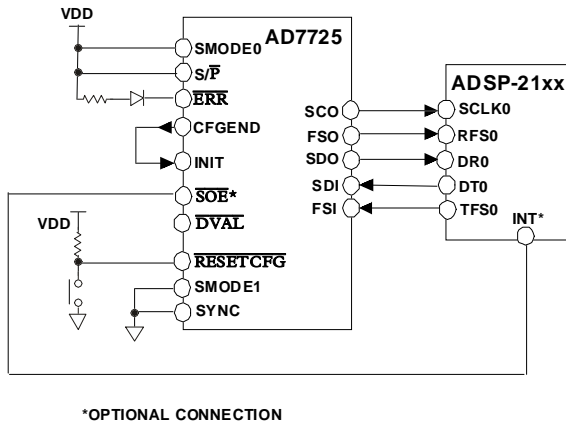


Figure 24. Loading the Configuration Data from a DSP.

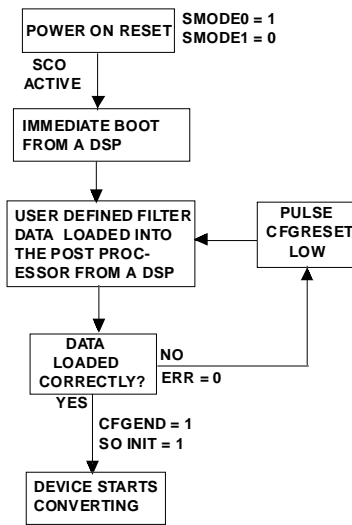


Figure 25. Flow Chart of DSP mode

Loading Configuration data from an External EPROM (EEPROM Mode)

In this mode, a filter can be developed off-chip by the user and the resulting configuration file is loaded into the post processor in the AD7725 from an External EPROM. The AD7725 therefore receives filter data from an EEPROM before outputting conversion results via the serial interface to a DSP. This mode of operation is selected by tying SMODE0 to ground and SMODE1 to V_{DD}. The values on these pins inform the AD7725 that user defined filter data is to be loaded from an external EPROM automatically on power up. Following power up the AD7725 will drive the \overline{SOE} pin low which will enable the EPROM and reset its pointer. The transfer of the configuration data will then commence with the data being latched into the AD7725 on the SCO rising edge. During the download

of data, SCO has a frequency of CLKIN/8. FSI is not used in the data transfer so is tied low. Once configuration is complete and no error occurred, \overline{SOE} will go high, disabling the EPROM; SCO will return to either CLKIN or CLKIN/2, depending on SCR; CFGEND will go high driving the INIT pin high and the device will start converting. However, if an error does occur during the configuration, the \overline{ERR} bit will go low and CFGEND will not go high. The part will not do anything until $\overline{RESETCFG}$ is pulsed low. When this occurs, the part is reset, \overline{SOE} goes low again to enable the EPROM and the part is reconfigured. Figure 26 shows the connection diagram for the AD7725 when loading configuration data from an EEPROM and figure 27 shows a flow chart of the powerup and configuration sequence.

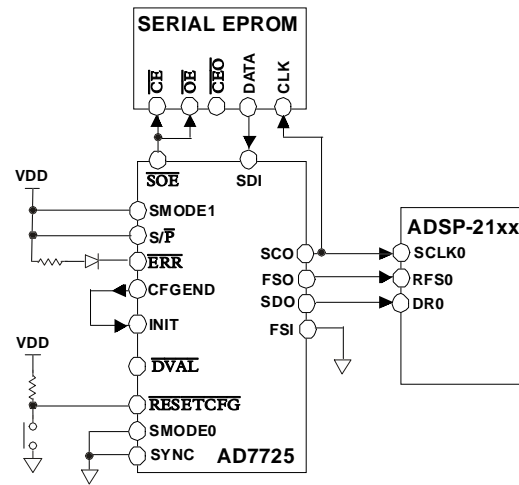


Figure 26. Loading the Configuration Data from an External EPROM

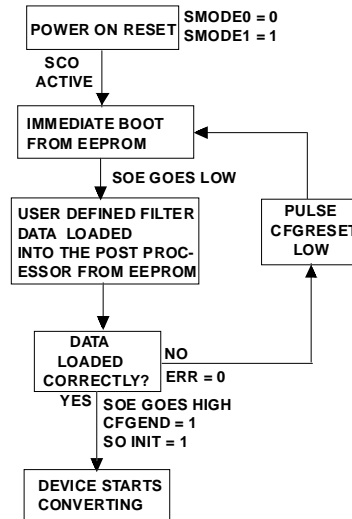


Figure 27. Flow Chart of EEPROM mode

Daisy Chaining Mode

Several AD7725s can be daisy-chained so that they are configured from a common external serial EPROM or a DSP and all conversion data is read back by a single DSP. When in Boot Mode (devices booting from a common EPROM), device 1 is configured then it sends the configuration data to device 2 via FSO/SDO to FSI/SDI.

When this device is configured, it sends the data onto the next device in the chain until all devices are configured. CFGEND of the last device is connected to INIT of all the devices so when the last device is configured, conversions are initiated (Conversion Mode).

When in Conversion Mode, the conversion result of device 1 is sent to the user register of device 2. The conversion result of device 2 is sent to the user register of the next device etc. A single DSP can read back the conversion data from all the devices in the sequence: device N; ... device 2; device1; device N; ... device 2; device1 etc. In order to have enough time to read back all the conversion data in one sampling period, the filters loaded into each device must decimate by at least N.

Therefore, to daisy-chain devices requires data to flow from device to device through SDO/FSO and SDI/FSI. A special configuration file is loaded into the devices to allow them to operate in this mode. Figure 28 illustrates how to cascade multiple devices with a common DSP and figure 29 shows how to cascade multiple devices with a common DSP and a shared EEPROM.

PARALLEL MODE

The parallel mode is selected by tying S/\bar{P} low. The parallel interface is a standard interface which interfaces to Digital Signal Processors and Microcontrollers. Pins $\overline{RD}/\overline{WR}$, \overline{CS} and \overline{RS} are used along with the data pins D0 to D15 to write instructions/configuration data and read the Status Register/conversion data. Figure 30 shows the interface between the AD7725 and a microprocessor.

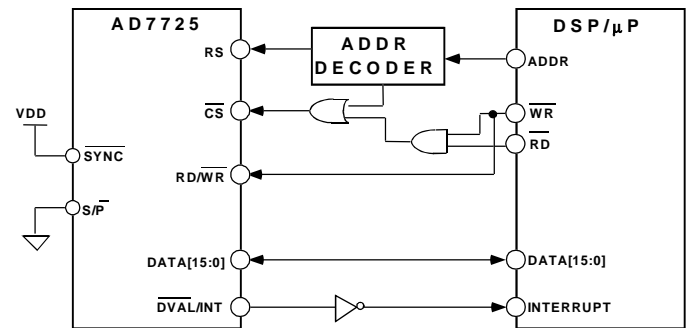


Figure 30. AD7725 Parallel Interface to Microprocessor.

During a read cycle, the RS pin informs the AD7725 whether the status register or a conversion result is being read. When RS is high, the status register is read while the data register, such as the device ID or a conversion result, is read when RS is low. Similarly, during a \overline{WR} cycle, an instruction is written when RS is high and data (such as configuration data) is written when RS is low. See table 2.

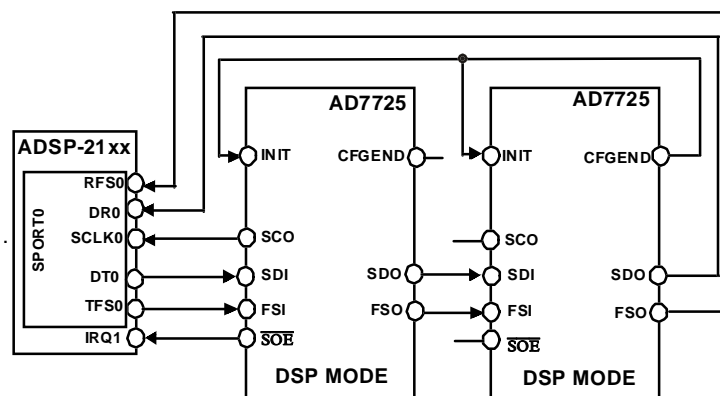


Figure 28. Daisy Chaining Devices with a Common DSP

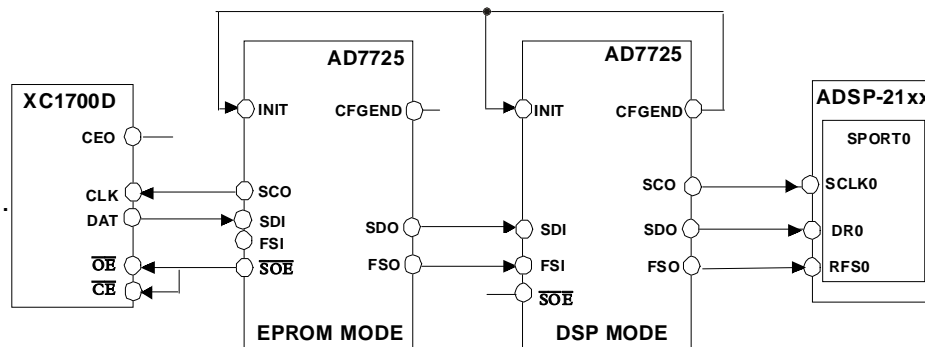


Figure 29. Daisy Chaining Devices with a Common DSP and a shared EEPROM

TABLE 2: READING AND WRITING

RD/ $\overline{\text{WR}}$ (pin 7)	RS (pin 4)	Operation
0	0	Write Data
0	1	Write Instruction
1	0	Read Data
1	1	Read Status Register

Parallel Mode Communication

The AD7725 provides two mechanisms by which a DSP or Microcontroller can communicate with it. These are:

(i) Interrupt Driven

The AD7725 relies on the issue of an interrupt to signal to the user that an action is required.

(ii) Polling the Status Register

The host processor interrogates the AD7725 to determine what to do next.

These two mechanisms would usually be combined for efficient communication. The status register may be read at any time.

Power on Reset

In parallel mode, an interrupt is issued at the completion of power on reset, indicating that the device is ready to communicate with the host processor. This interrupt is cleared by reading the Status Register or writing an instruction.

Configuration Data Format

Every configuration file contains a device identification word (ID) unique to the AD7725. They also have CRC (cyclic redundancy check) flags every 42 words throughout the file. These are used by the device to ensure that the file is of the correct format and that it has not been corrupted. Errors in the configuration file will cause interrupts (unless they are masked) which will show up in the Status Register. The device ID may be read by issuing the RdID instruction (see table 4).

Configuring the Device

After power on reset, the AD7725 can either be configured by its internal default filter or from an external source via the parallel interface. Three instructions are provided for configuring the AD7725 (see table 4).

(i) BFR (Boot from ROM) - This instruction will inform the device to load the configuration data of the default filter, stored in internal ROM.

If the device is to be configured from an external source via the parallel interface, the following two instructions determine the way in which this done:

(i) WrConfig (Write Configuration)

When this instruction is issued, the device will generate an interrupt every time a new word of the configuration data is required. The interrupt is cleared on the falling edge of $\overline{\text{CS}}$ during the data write cycle. This continues until the complete file is written. Immediately after the last word of the configuration data is written, a final interrupt is asserted to indicate 'Instruction Done'.

However, if an error occurred during the configuration process, if the configuration data is corrupt or in the wrong format, an error will occur and an interrupt will be asserted.

It is advised that when using this instruction, the Status Register is read after each interrupt to ensure no errors occurred and that the correct response is made. If configuration data is corrupt, it will not be internally written to the post processor.

(ii) WrConfigEM (Write Configuration with Error Mask)

When this instruction is issued, no interrupts to signal errors will ever be asserted during the download of the configuration file. This saves reading the Status Register in response to every interrupt as with the previous instruction.

The configuration process will always run through 512 data write cycles, then the 'Instruction Done' interrupt is issued. In this case, the Status Register should be checked at the end of the configuration to verify whether errors occurred during the configuration. If configuration data is corrupt, it will not be internally written to the post processor.

Reading the Status Register

To read the status register, RS is taken high and RD/ $\overline{\text{WR}}$ is taken high. When $\overline{\text{CS}}$ is taken low, the contents of the status register will be output. The status register is shown in Table 3.

Converting

To begin conversions, the RdCONV (Read Converter Data) instruction is issued (see table 4). INT is asserted as soon as the conversion data is ready to be read (bit 14 of the status register will be set). INT will remain high until the digital word is read from the device. It will then go low and return high when the next conversion is complete.

The device continues to convert until the ABORT instruction is issued.

TABLE 3: STATUS REGISTER

Bit	Name	Function
15	InstrBUSY	This bit is set to 1 when an instruction is being performed.
14	Data Ready	This bit is set to 1 when data is ready to be read from the device (i.e. a Read Data cycle is required)
13	Data Request	This bit is set to 1 when the device requires data to be written to it (i.e. a Write Data cycle is required).
12	ID Error	This bit is set to 1 if the programming data has an incorrect ID Value.
11	CRC Error	This bit is set to 1 if Corrupt Data is loaded into the Device.
10	Data Error	This bit is set to 1 if an overflow occurs to indicate that the conversion result is invalid.
9	InstrReg[15]	Instruction Register Bit 15
8	InstrReg[13]	Instruction Register Bit 13
7	InstrReg[12]	Instruction Register Bit 13
6	InstrReg[11]	Instruction Register Bit 11
5	InstrReg[6]	Instruction Register Bit 6
4	InstrReg[5]	Instruction Register Bit 5
3	InstrReg[4]	Instruction Register Bit 4
2	InstrReg[1]	Instruction Register Bit 1
1	InstrReg[0]	Instruction Register Bit 0
0	CFGEND	Configuration End Flag. This is set to 1 when the device has been configured correctly and is ready to start converting.

TABLE 4. INSTRUCTION SET

Instruction	Hex Code	Description
BFR	0x2800	Boot From Internal ROM.
RdID	0x8802	Read Device ID.
RdCONV	0x8D21	Read Converter Data. When this instruction is issued to the AD7725, the device will continue to output conversion data until the ABORT instruction is issued.
WrConfig	0x3000	Write Configuration Data.
WrConfigEM	0x3200	Write Configuration Data, Mask Errors.
ABORT	0x0000	Abort. This instruction is a soft reset i.e. it breaks the conversion process and leaves the device in a clean state, still configured, ready for the next instruction.

GROUNDING AND LAYOUT

The analog and digital power supplies to the AD7725 are independent and separately pinned out to minimize coupling between analog and digital sections within the device. All the AD7725 AGND and DGND pins should be soldered directly to a ground plane to minimize series inductance. In addition, the ac path from any supply pin or reference pin (REF1 and REF2) through its decoupling capacitors to its associated ground must be made as short as possible (Figure 31). To achieve the best decoupling, place surface mount capacitors as close as possible to the device, ideally right up against the device pins.

All ground planes must not overlap to avoid capacitive coupling. The AD7725's digital and analog ground planes must be connected at one place by a low inductance path, preferably right under the device. Typically, this connection will either be a trace on the Printed Circuit Board of 0.5 cm wide when the ground planes are on the same layer, or 0.5 cm wide minimum plated through holes when the ground planes are on different layers. Any external logic connected to the AD7725 should use a ground plane separate from the AD7725's digital ground plane. These two digital ground planes should also be connected at just one place.

Separate power supplies for AV_{DD} and DV_{DD} are also highly desirable. The digital supply pin DV_{DD} should be powered from a separate analog supply, but if necessary DV_{DD} may share its power connection to AV_{DD}.

A minimum etch technique is generally best for ground planes as it gives the best shielding. Noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals and, both should be kept away from digital signals. In waveform sampling and reconstruction systems, the sampling clock (CLKIN) is as vulnerable to noise as any analog signal. CLKIN should be isolated from the analog and digital systems. Fast switching signals like clocks should be shielded with their associated ground to avoid radiating noise to other sections of the board and, clock signals should never be routed near the analog inputs.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7725 to shield it from noise coupling. The power supply lines to the AD7725 should use as large a trace as possible (preferably a plane) to provide a low impedance path and reduce the effects of glitches on the power supply line. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the affects of feedthrough through the board.

TBD

Figure 31. Reference and Supply Decoupling

**OPTIMIZING HEAT REMOVAL BY PCB
CONSTRUCTION AND DEVICE MOUNTING**

For normal still air conditions, the primary heat dissipation path from the chip to the ambient is via the component leads into the PCB. The thermal resistance of the board is then a significant variable. This can be lowered by maximising the use of ground planes as heat sinks and also by optimising the way in which the heat can be dissipated, for example conduction into the board mounting chassis. The greater the percentage of copper in the board, especially in the region of the device, the lower the thermal resistance. The use of wide tracks and thermal vias to the ground plane will have a significant effect. Placing critical components close to where the edge of the board is attached to the chassis can provide additional cooling without the use of heatsinks or forced air. Avoid close spacing of high power devices, in order to ensure that the heat is dissipated over the maximum possible area.